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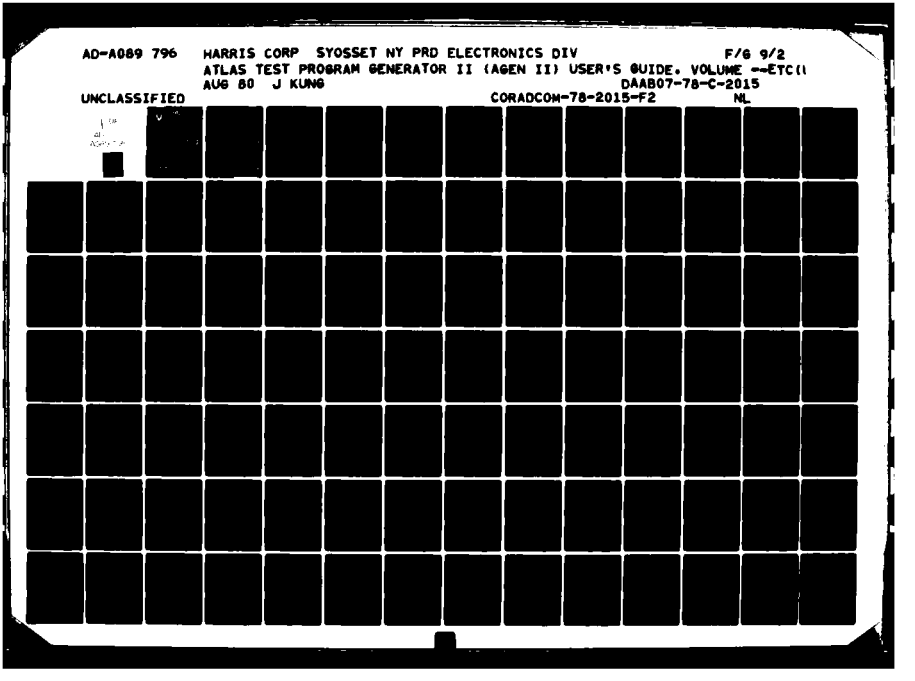

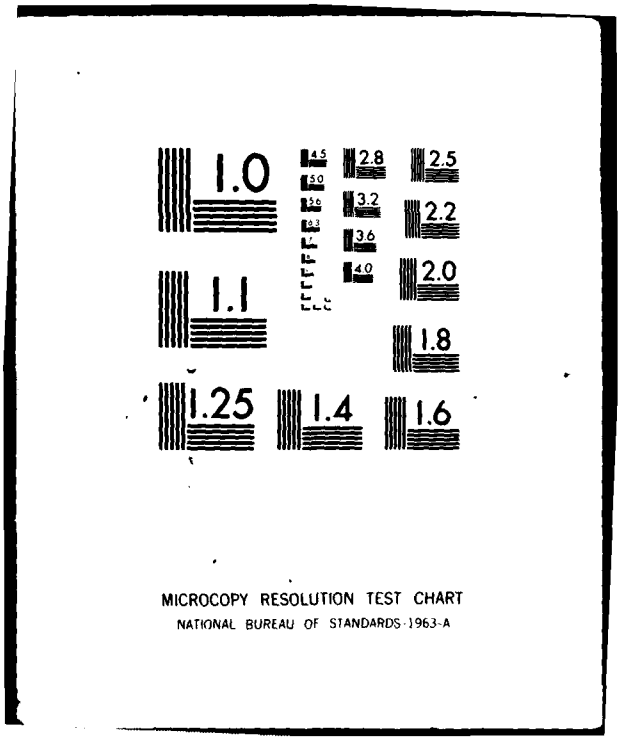
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LEVEL II

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
CORADCOM-78-2015-F2

ATLAS TEST PROGRAM GENERATOR II (AGEN II)
User's Guide—Volume II

Jeffrey Kung
PRD Electronics Division
HARRIS CORPORATION
Syosset, New York 11791

August 1980

Final Report for Period April 1978—August 1980

Prepared for:
CENTER FOR TACTICAL COMPUTER SYSTEMS

CORADCOM
US ARMY COMMUNICATIONS RESEARCH & DEVELOPMENT COMMAND
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Automatic Test Program Generation
Automatic Test Equipment
Test, Measurement and Diagnostic Equipment

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This is the final report on the Army-CORADCOM-sponsored project which, had as its objective, the design and implementation of a software processor which would automate the process of generating source code for test programs of various linear analog circuits. The approach used by AGEN (ATLAS Generator) is to take one type of linear analog circuit, e.g., amplifier, and subject it to an in-depth circuit analysis to determine the commonalities among similar types of circuits. Once the

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commonalities are defined, a circuit model is structured by ATLAS test language through common data base FORTRAN software techniques. The resultant ATLAS model source program is basically a standardized, high quality, error-free ATLAS test progra with the variables opened as windows for the AGEN users to insert the values for their individual test specifications. Therefore, the AGEN program is an interactive test program which requires only test specifications from the user to complete the program generation.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONT'D)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Contd)

INTRODUCTION

The ATLAS Generator (AGEN) System is a computer program system used for the automatic source code generation of ATLAS test programs for functional testing of analog Units Under Test (UUT's) with minimum basic information demand from the AGEN user.

AGEN is a FORTRAN Executive Program which accesses a Library that contains ATLAS source test routines in card image.

Equipped with a list of parameters the operator interacts with the executive by answering questions presented on the CRT screen. The introductory questions elicit the type of network and the desired characteristics. In response, AGEN requests specific parameters that are necessary for the test run. When all questions have been answered, AGEN will call up a source deck, insert the parameters, and write the source out to a file. The program can then be compiled and run on the ATE.

The AGEN executive program does all the work of interactively obtaining the input parameter list from the operator, performing necessary calculations, and generating the output list required by the ATE source program. This is shown in figure 1-1. However, the procedure to go from the input list to the final end product of an ATE object tape capable of being run on station is described in Section II.

The details associated with AGEN II UUT's are covered in Sections II through IV. Section II explains test philosophy and mathematical equations associated with each network characteristic. It also provides the Interface Device (ID) design for each test. Section III contains the test flow chart for each network characteristic of the UUT. Section IV shows the schematics of each UUT. Section V contains the diagram and schematic of the ID. Section VI describes the MODEM system which allows remote connection of the EQUATE to PRD resident AGEN source program generator. Section VII consists of all test data recorded during the AGEN II project validation performed at Army Depot, Tobyhanna, PA, on May 1, 1980.

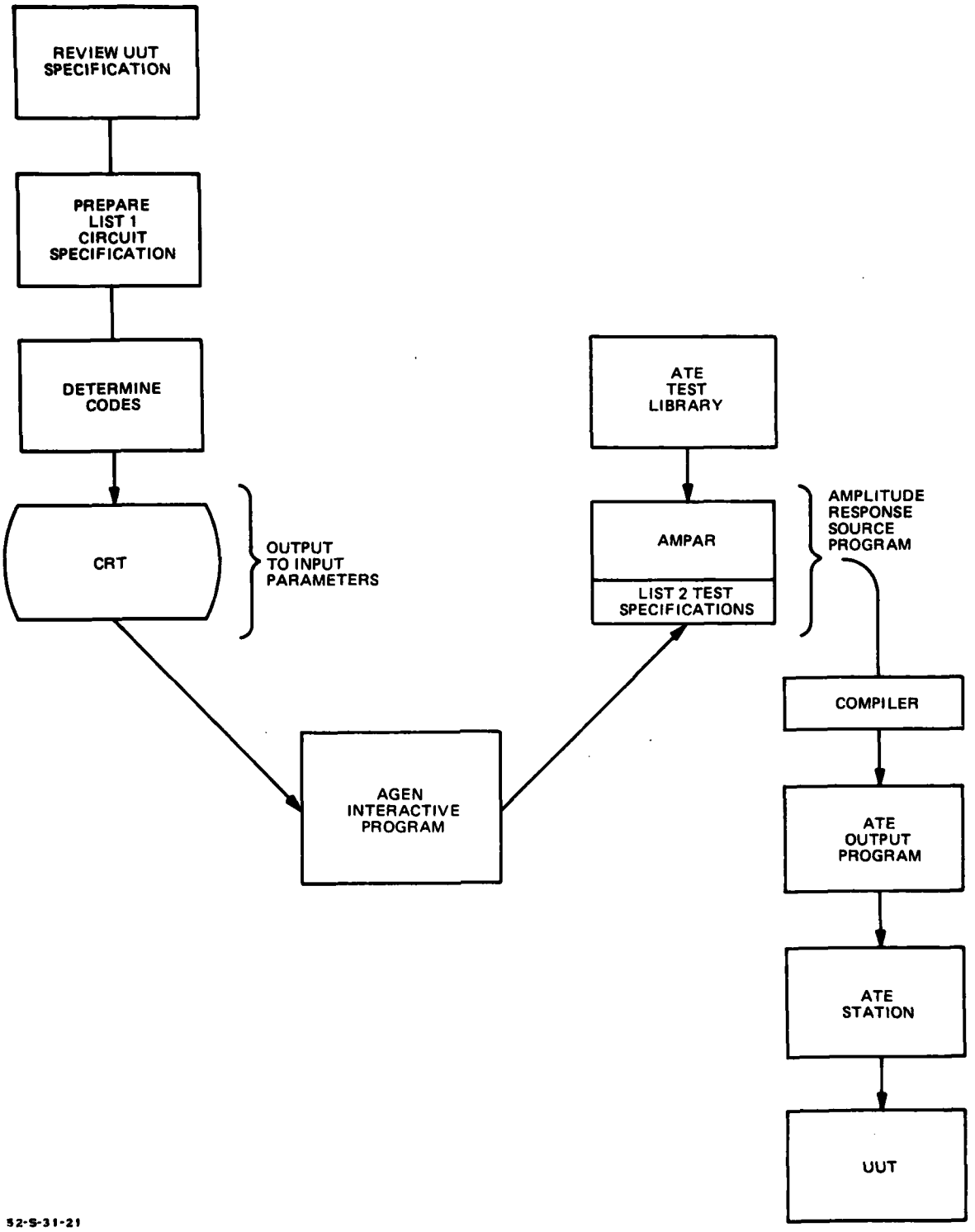


Figure 1-1 AGEN Information Flow Block Diagram

SECTION I.

AGEN II OPERATIONAL PROCEDURE

1.1 TEST PROCEDURE

In order to create a test program under AGEN, the user must perform the following steps.

(1) Examine the circuit. Note the network class it belongs to, e.g., amplifier, oscillator, power supply, mixer, or filter. Refer to paragraph 1.2.1.

(2) Determine which characteristics are to be tested, e.g., linearity, harmonic distortion, etc. Refer to paragraph 1.2.2.

(3) Design the ID according to the respective ID diagram. Refer to Section II.

(4) Interact with the AGEN executive, inserting the parameters by answering the questions. AGEN will complete the task. It will take the input parameters, perform necessary calculations, enter test specifications to the ATE source program, and then output the ATE source program to the disc.

(5) The user will now compile the test program and test the circuit on the ATE station.

1.2 NETWORK AND CHARACTERISTIC CODES

1.2.1 Network Codes

Code	Description
1	Amplifier
2	Oscillator
3	Power Supply
4	Mixer
5	Filter

1.2.2 Characteristic Codes

For N=1 (Amplifier)

Code	Description	ATLAS Source Title
1	Amplitude Response	AMPAR
2	Linearity	AMPLN

For N=2 (Oscillator)

Code	Description	ATLAS Source Title
1	Frequency Stability	OSCFS
2	Amplitude Stability	OSCAS

For N=3 (Power Supply)

Code	Description	ATLAS Source Title
1	Regulation	PWSREG
2	Ripple	PWSRPL
3	Over Current	PWSOVC

For N=4 (Mixer)

Code	Description	ATLAS Source Title
1	Isolation	MIXISO
2	Frequency Response	MIXFRS
3	Conversion Loss	MIXCON

For N=5 (Filter)

Code	Description	ATLAS Source Title
1	Insertion Loss	FILILO
2	Phase Response	FILPHR
3	Input Impedance	FILINZ
4	Output Impedance	FILOUZ
5	Amplitude Response	FILAMR

1.3 AGEN OPERATION (NOTE: Depress CONTROL-F key on the background terminal to disable the foreground terminal)

(1) Enter the following command into the BACKGROUND terminal.

COMMO ↵ NOTE: "↵" represents the carriage return key

(2) Dial (516)364-0840 and insert the Handset into the Acoustic Coupler.

(3) Enter the following command into the FOREGROUND terminal.

UICKEN)

the computer will respond by displaying

UNIVAC 1100 OPERATING SYSTEM VER.33R3/PRD-33(RSI)

(4) Enter the following command

@RUN AGEN,PRDARC,AGEN)

(NOTE: PRD ARC is the account number)

the computer will respond by displaying

DATE: ØØØØØØ TIME: ØØØØØØ

(5) Enter the following command

@ASG,A AGEN2.)

the computer will respond by displaying

READY

(6) Enter the following command

@AGEN2.AGEN)

the AGEN program will generate questions on the screen for the operator who will supply the technical specifications for the UUT. More than one test can be run at one time (e.g., amplifier response, linearity, oscillator frequency stability etc)

(7) As an example, the following list of questions and answers has been taken from an actual AGEN run. The network is 1 (amplifier) and the characteristic is 1(amplitude response). The operator's responses have been underlined.

(8) At the end of the questions, the AGEN program will automatically call up the ATLAS programs in card image and insert the data into the corresponding blanks. The ATLAS source programs will be saved on the disc in consecutive files labeled TAPEØØ., TAPEØ1., TAPEØ2. ---- TAPENN., where TAPEØØ. is the first ATLAS source file and TAPENN. is the last ATLAS source file generated by the AGEN.

```
@AGEN2.AGEN

                PRD  ELECTRONICS
              SYOSSET, N.Y., 11791
         ( A DIVISION OF HARRIS CORPORATION )

              ----------------------
                ATLAS   GENERATOR
              ----------------------

THIS PROGRAM PERFORMS COMPUTER AIDED TEST GENERATION
FOR FUNCTIONAL TESTING OF ANALOG UNITS IN LINEAR RANGE .


PLEASE TYPE YOUR NETWORK (N) CODE OR H FOR HELP
>1 )


PLEASE TYPE (C) CODE FOR THIS CHARACTERISTIC TO BE TESTED
OR H FOR HELP.  TYPE IN ALL IF ALL CODES ARE TO BE TESTED.
>1 )
PLEASE TYPE NEXT C CODE IF ANY, OR G TO GO ON
>G )


 ------------------------------------------------------
            SELECTED UUT SPECIFICATIONS
 ------------------------------------------------------
    MAIN CATEGORY          AMPLIFIERS
    CHARACTERISTICS        AMPLITUDE RESPONSE
 ------------------------------------------------------


ARE SPECIFICATIONS CORRECT.  TYPE Y FOR YES, N FOR NO
>Y )

THE FOLLOWING QUESTIONS PERTAIN TO AMPLIFIER - AMPLITUDE RESPONSE

TYPE IN DC SUPPLY REQUIRED FOR THE UUT IN VOLTS AS XX.X
(RANGE: 0 TO 36 VOLTS.)
>9.5 )


THE FOLLOWING TEST FREQUENCY RANGES ARE AVAILABLE:

    (1) 2 HZ TO 1 MHZ

    (2) 60 KHZ TO 100 MHZ

PLEASE TYPE IN TEST FREQUENCY RANGE CHOICE 1 TO 2.
>1 )

THE SELECTED RANGE IS 2 TO 1000000.
```

(1) REFER TO ID DIAGRAM.

(2) SINEWAVE FROM WAVEFORM GENERATOR 50 OHMS OUTPUT IMPEDANCE IS USED AS THE SIGNAL SOURCE.

(3) TRMS VOLTMETER HI INPUT IMPEDANCE IS USED AS THE MEASURING DEVICE.

TYPE IN UUT INPUT VOLTAGE IN MILLIVOLTS RMS FROM WAVEFORM GENERATOR TO ID (50 OHM LOAD) (MVRMS) AS XXXX.X
(RANGE: 0 TO 2400 MVRMS)
>35.

TYPE IN FIVE (5) FREQUENCIES IN HZ AS XXXXXXX.X IN ASCENDING ORDER.
(RANGE: 2 HZ TO 1 MHZ.)

F1 =
>600.

F2 =
>900.

F3 =
>1200.

F4 =
>1500.

F5 =
>2000.

TYPE IN THE INSERTION LOSS IN DB OF THE UUT INPUT MATCHING NETWORK IN THE ID AS XX.X DB.
RANGE 0.0 - 99.9
>0

TYPE IN THE INSERTION LOSS IN DB OF THE UUT OUTPUT MATCHING NETWORK IN THE ID AS XX.X DB.
RANGE 0.0 - 99.9
>3.

TYPE IN NOMINAL GAIN WITHIN THE UUT FREQUENCY BAND IN DB AS XXX.XX
(RANGE: 0 TO 999.99 DB.)
>29.

TYPE IN NOMINAL GAIN DEVIATION FORMAT AS FOLLOWS:

(1) FIXED % OF NOMINAL GAIN.

(2) FIXED ABSOLUTE VALUE.

>2

TYPE IN NOMINAL GAIN DEVIATION ABSOLUTE VALUE IN DB AS XX.XX
(RANGE: 0 TO 99.99 DB)
>2.

USER SELECTED PARAMETERS

#	PARAMETERS	VALUES	UNIT
1	DC SUPPLY	9.5	VOLTS
2	FREQUENCY RANGE CHOICE	1	
3	INPUT VOLT FROM GEN.	35.0	MVRMS
4	F1	600.0	HZ
5	F2	900.0	HZ
6	F3	1200.0	HZ
7	F4	1500.0	HZ
8	F5	2000.0	HZ
9	NOMINAL GAIN	29.00	DB
10	NOM. GAIN DEV. FORMAT	2	
11	NOM. GAIN DEV. %	.00	%
12	ABSOLUTE NOM. GAIN DEV.	2.00	DB
13	INSERTION LOSS OF INPUT	.00	DB
14	INSERTION LOSS OF OUTPUT	3.00	DB

ARE SELECTED PARAMETERS CORRECT ? TYPE IN Y FOR YES, N FOR NO.

>Y

THE FOLLOWING AUTOMATICALLY GENERATED ATLAS PROGRAM
WILL TEST THE USER SELECTED AMPLIFIER AT THE USER
SPECIFIED PARAMETERS .

```
C BOT                                                                   $
C       AMPLIFIER AMPLITUDE RESPONSE TEST.FILE NAME 'AMPAR' $
        DECLARE DECIMAL, 'VMAX','Y','INDB','DBMX' $
        DECLARE DECIMAL,LIST,'F'(5), 'OPT'(5),
                           'MDBI'(5),'MDBO'(5),'GAIN'(5) $
C           CCCCC1                                                      $
        DEFINE 'VDC',                  9.5                              $
        DEFINE 'FCHOICE',                1                              $
        DEFINE 'VIN',                 35.0                              $
        DEFINE 'DBIN',                   0                              $
        FILL'F', (1)                 600.0                              ,
                 (2)                 900.0                              ,
                 (3)                1200.0                              ,
                 (4)                1500.0                              ,
                 (5)                2000.0                              $
        DEFINE 'GNUL',               31.00                              $
        DEFINE 'GNLL',               27.00                              $
        DEFINE 'MATCHIN',                0                              $
        DEFINE 'MATCHOT',              3.0                              $
C       PROCEDURAL SECTION $
E  1000 COMPARE 'FCHOICE', GT 1.5 $
        GOTO STEP 1010 IF GO $
C       GAIN MEASUREMENT, FREQUENCY RANGE 2HZ TO 1MHZ $
       'DISPLAY,'PERFORM HOOKUP AS FOLLOWS.PRESS PROCEED WHEN COMPLETE.
                 ID-BOX         TABLE-TOP
                 UUT I/P        J[illegible]
                 UUT O/P        J[illegible]
                 UUT PWR I/P    J29
                 INSERT UUT INTO THE UUT CONNECTOR OF THE [illegible]
```

```
          WAIT-FOR MANUAL-INTERVENTION $
C         APPLY DC2A OUTPUT TO UUT DC-POWER INPUT $
          APPLY DC-SIGNAL DC2A, VOLTAGE 'VDC'V $
          DELAY 100 MSEC $
C         MEASUREMENT OF UUT OUTPUT VOLTAGE FOR FIVE FREQUENCIES $
          FOR 'Y'=1 THRU 5 THEN $
          APPLY AC-SIGNAL, SINE-WAVE, FREQ 'F'('Y')HZ, VOLTAGE 'VIN'MV,
          TEST-EQUIP-IMP 500HM, UUT-IMP 500HM $
          'INDB'= 20*LOG('VIN'/224) $
          'DBMX' = ('DBIN'+'GNUL')-('MATCHIN'+'MATCHOT') $
          'VMAX' = ALOG('DBMX'/20)*2.0 $
          MEASURE(VOLTAGE-TRMS 'OPT'('Y')MV),AC-SIGNAL, AC-COUPLE,
          VOLTAGE-TRMS MAX'VMAX'MV, FREQ MAX 'F'('Y')HZ,
          DELAY 100MSEC, CNX BNC 1 $
          END FOR $
          REMOVE AC-SIGNAL $
          REMOVE DC2A $
C         CALCULATION OF MEASURED GAIN IN DB $
          FOR 'Y'= 1 THRU 5 THEN $
          'GAIN'('Y')= 20*LOG('OPT'('Y')/'VIN')+('MATCHIN'+'MATCHOT') $
          END FOR $
          GOTO STEP 1020 $
C         GAIN MEASUREMENT, FREQUENCY RANGE   >1MHZ TO 100MHZ $
     1010 DISPLAY,"PERFORM HOOKUP AS FOLLOWS.PRESS PROCEED WHEN COMPLETE.
                   ID-BOX          TABLE-TOP
                   UUT I/P         J13
                   UUT O/P         J37
                   UUT PWR I/P     J29
                   INSERT THE UUT INTO THE UUT CONNECTOR ON THE ID-BOX" $
          WAIT-FOR MANUAL-INTERVENTION $
C         APPLY DC2A OUTPUT TO UUT DC-POWER INPUT $
          APPLY DC-SIGNAL DC2A, VOLTAGE 'VDC'V $
          DELAY 100MSEC $
C         MEASUREMENT OF UUT OUTPUT FOR FIVE INPUT FREQUENCIES $
          FOR 'Y'=1 THRU 5 THEN $
          APPLY RF-SIGNAL RFB, FREQ 'F'('Y')KHZ, POWER 'DBIN'DBM $
          'DBMX'=('DBIN'+'GNUL')-('MATCHIN'+'MATCHOT') $
          'VMAX' =224* ALOG('DBMX'/20)* 1.5 $
          MEASURE (VOLTAGE-TRMS 'OPT'('Y')MV),AC-SIGNAL,AC-COUPLE,
          VOLTAGE-TRMS MAX 'VMAX'MV,FREQ MAX 'F'('Y')KHZ,TEST-EQUIP-IMP 500HM,
          DELAY 100MSEC, CNX BNC 1$
          END FOR $
          REMOVE RFB $
          REMOVE DC2A $
C         CONVERT MEASURED VALUES INTO DBM AND CALCULATE GAIN IN DB $
          FOR 'Y'=1 THRU 5 THEN $
          'MDBO'('Y')=20*LOG('OPT'('Y')/224) $
          'GAIN'('Y')= 'MDBO'('Y')+'MATCHOT'+'MATCHIN'-'DBIN' $
          END FOR $
C         RECORD MEASURED DATA $
          RECORD, "     " $
     1020 RECORD'OPT'(1),"MEASURED OUTPUT VOLTAGE1= ######MV" $
          RECORD'OPT'(2),"MEASURED OUTPUT VOLTAGE2= ######MV" $
          RECORD'OPT'(3),"MEASURED OUTPUT VOLTAGE3= ######MV" $
          RECORD'OPT'(4),"MEASURED OUTPUT VOLTAGE4= ######MV" $
          RECORD'OPT'(5),"MEASURED OUTPUT VOLTAGE5= ######MV" $
          FOR 'Y'=1 THRU 5 THEN $
          COMPARE 'GAIN'('Y'),UL 'GNUL'LL 'GNLL' $
          GOTO STEP 1030 IF NOGO $
```

```
          END FOR $
          RECORD, "     " $
          RECORD,"UUT PASSED AMPLITUDE RESPONSE TEST" $
          GOTO STEP 1040 $
     1030 RECORD,"UUT FAILED AMPLITUDE RESPONSE TEST" $
          RECORD, "     " $
     1040 RECORD'GAIN'(1),"TEST1.MEASURED GAIN= ###.##DB" $
          RECORD'GAIN'(2),"TEST2.MEASURED GAIN= ###.##DB" $
          RECORD'GAIN'(3),"TEST3.MEASURED GAIN= ###.##DB" $
          RECORD'GAIN'(4),"TEST4.MEASURED GAIN= ###.##DB" $
          RECORD'GAIN'(5),"TEST5.MEASURED GAIN= ###.##DB" $
          RECORD, "     " $
          RECORD'GNUL','UPPER LIMIT OF GAIN = ###.##DB" $
          RECORD'GNLL','LOWER LIMIT OF GAIN = ###.##DB" $
          REMOVE ALL $
          FINISH $
          TERMINATE $
C EOT      $
C     $


DO YOU WANT TO DO ANOTHER NETWORK ?
PLEASE TYPE IN Y FOR YES, N FOR NO .


>N

DO YOU WISH THE ATLAS PROGRAM WRITTEN TO TAPE??
PLEASE TYPE "Y" FOR YES, AND "N" FOR NO
>N


YOU HAVE COMPLETED AUTOMATIC ATLAS PROGRAMS GENERATION .

THANK YOU FOR SPENDING  1.22 SECONDS WITH AGEN .

GOOD LUCK AT YOUR TEST STATION !!



>@FIN
```

(9) The computer will ask if the user would also like to generate a backup ATLAS source tape on the UNIVAC 1108 system. Answer by typing
NO ⟩ or YES ⟩
the computer will display the ATLAS programs names that have been written on the disc by the AGEN. It will also display the computer time spent by the user.

(10) Enter the following command to sign-off the UNIVAC 1108.
@FIN ⟩
the computer will respond by displaying a sign-off message.

(11) Enter the following command to disconnect the terminal
@@TERM ⟩
the carrier detect light on the Acoustic Coupler will go off.

(12) To return the system under RDOS control, enter the following command at the BACKGROUND terminal
CTRL-A (Control key and letter A key depressed at the same time).
the computer will respond by displaying the letter R.

(13) The ATLAS source files on the disc can now be compiled and transferred to the tape by the standard CLI commands.

NOTE: To return the Program Development Center (PDC) to its normal operating condition, re-boot the Run Time System.

SECTION II.

AGEN II NETWORK/CHARACTERISTIC DESCRIPTION

2.1 AMPLIFIER AMPLITUDE RESPONSE TEST

Amplifier amplitude response is the measurement of gain when the frequency of the applied signal is varied. The amplitude of the applied signals is kept constant in all the measurements. The gain should stay within certain limits over the UUT frequency range. The UUT's in AGEN are divided into two groups according to their frequency range.

2.1.1 FREQ. RANGE 2 HZ - 1 MHZ

The AGEN user designs the Interface Device (ID) according to the ID diagram (fig. 2.1). Matching networks of known insertion loss, as indicated in the ID diagram, may be required in the ID design. The user will then enter the following parameters to the AGEN to generate the UUT test program.

- DC power input
- Frequency range (2HZ-1MHZ or 60KHZ-100MHZ)
- Input voltage(from waveform generator to ID as UUT input)
- Five frequencies(within the UUT frequency range)
- Nominal gain(DB)
- Permissible deviation in gain (AGEN will compute the upper and lower limits of gain measurements)
- Insertion loss(DB of the UUT input and output matching networks)

At the execution of the UUT test program, UUT output is measured for each frequency input by the TRM's voltmeter (Hi Z Input). Gain in DB is then calculated automatically at each frequency using the following equation.

$$GAIN(DB) = 20 \log (OPT/VIN) + (MATCHIN + MATCHOT)$$

where OPT = Measured output in millivolts RMS

VIN = Applied input millivolts RMS

MATCHIN = Insertion loss in DB of the input matching network

MATCHOT = Insertion loss in DB of the output matching network

The measured gain is compared with the upper and lower limits for the test FAIL/PASS decision.

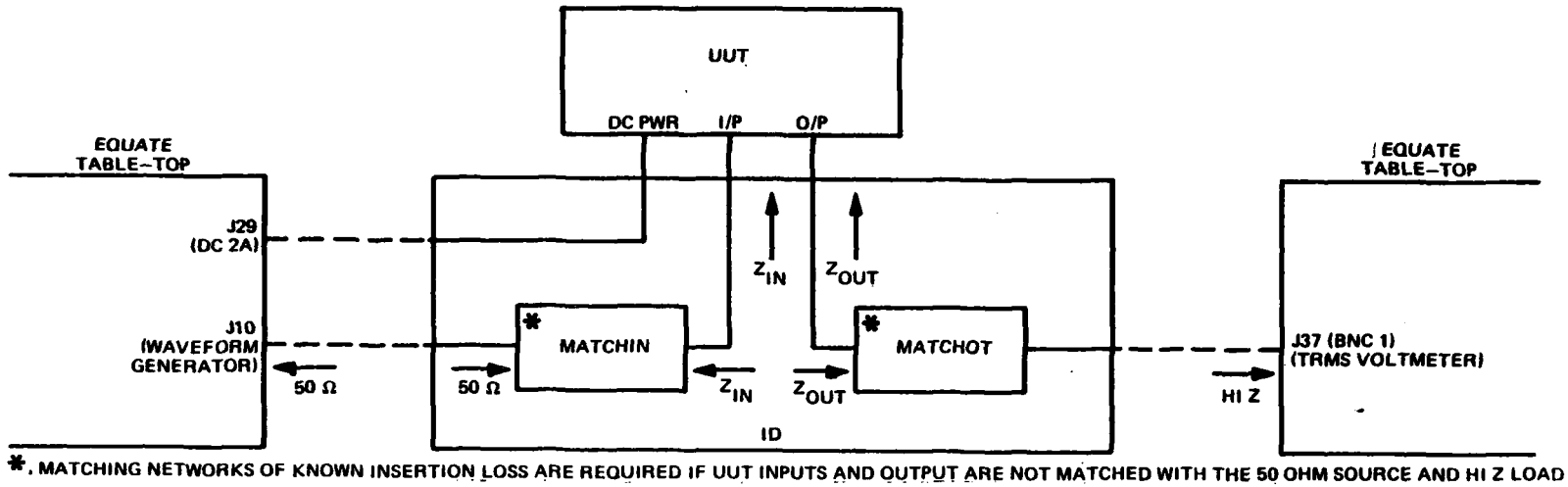


Figure 2-1. ID Diagram: Amplifier Amplitude Response Test - Frequency 2 Hz - 1 MHz

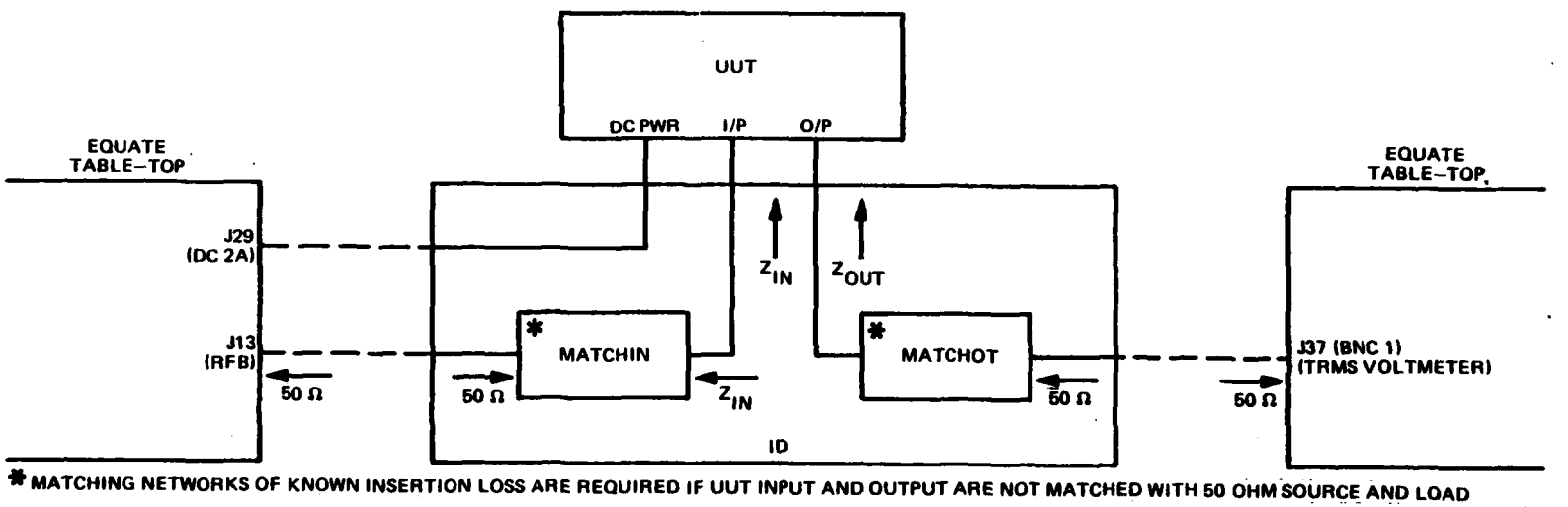


Figure 2-2. ID Diagram: Amplifier Amplitude Response Test - Frequency 60 kHz - 100 MHz

2.1.2 Freq. Range 60 KHZ - 100 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2.2). Matching networks of known insertion loss as indicated in the ID diagram may be required in the ID design. The parameters entered to AGEN are the same as above except the input voltage to UUT is entered in DBM (RFB is used as the signal source).

At the execution of the UUT test program UUT output is measured for each frequency input using the TRMS voltmeter (50Ω Zin). The measured values are converted automatically into DBM using the following equation.

MDBO = 20 LOG (OPT/224)

where MDBO = Measured output in DBM

OPT = Measured output in millvolts RMS

Gain is automatically calculated for each frequency input using the following equation.

GAIN(DB) = MDBO + MATCHOT + MATCHIN - DBIN

where MDBO = output in DBM calculated above

MATCHOT = Insertion loss in DB of the output matching network

MATCHIN = Insertion loss in DB of the input matching network

DBIN = Applied signal in DBM from RFB to ID as UUT input.

The measured gain is compared with the upper and lower limits for the test FAIL/PASS decision.

2.2 AMPLIFIER LINEARITY TEST

Amplifier linearity is the variation in gain when the amplitude of the applied signal to UUT is varied. The frequency of the applied signal is kept constant in all the measurements. The gain should stay within certain limits over the UUT linear range. The UUT's in AGEN are divided into two (2) groups according to their frequency range.

2.2.1 Freq. Range 2 HZ - 1 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-3), Matching networks of known insertion loss as indicated in the ID diagram, may be required in the ID design. The user will then enter the following parameters to the AGEN to generate the UUT test program.

- DC power input
- Frequency range (2 HZ - 1 MHZ or 60 KHZ - 100 MHZ)

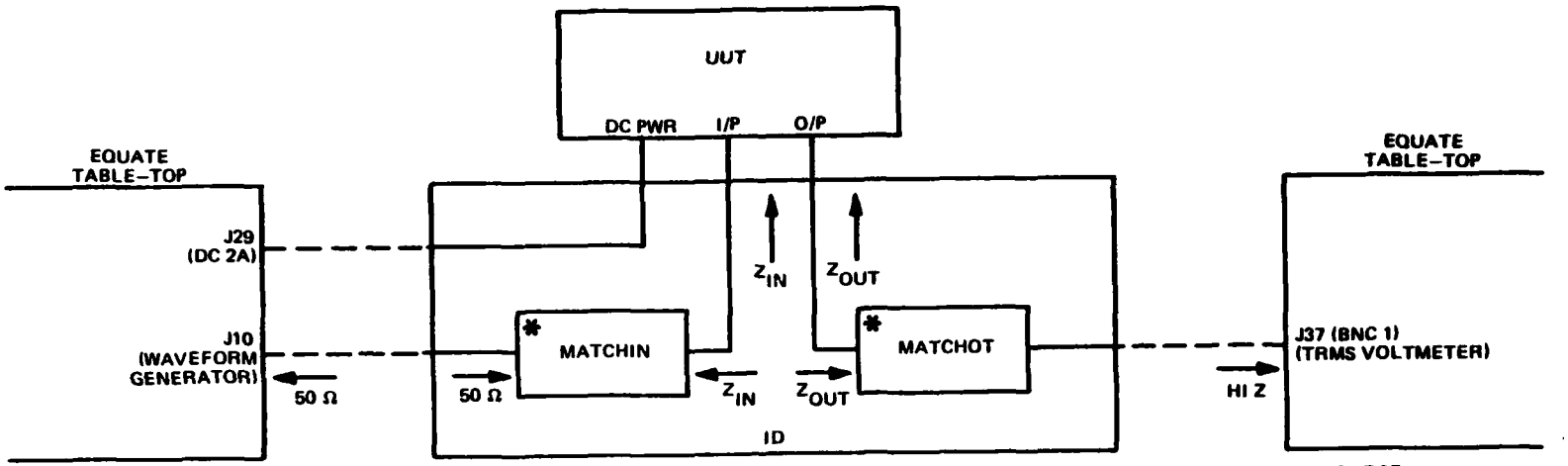


Figure 2-3. ID Diagram: Amplifier Linearity Test - Frequency 2 Hz - 1 MHz

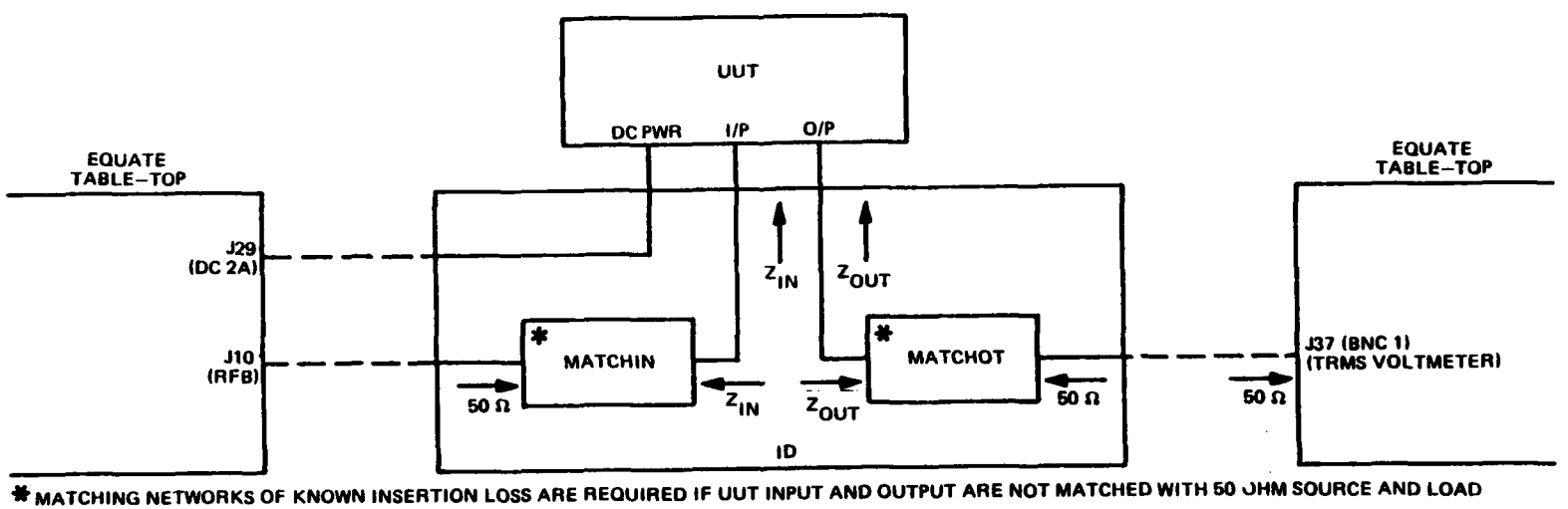


Figure 2-4. ID Diagram: Amplifier Linearity Test - Frequency 60 kHz - 100 MHz

- Five input voltages (from waveform generator to ID as UUT inputs)
- Midband frequency
- Nominal gain (DB)
- Permissible deviation in gain (AGEN will compute the upper and lower limits of gain measurements)
- Insertion loss (DB of the UUT input and output matching networks)

At the execution of the UUT test program, UUT output is measured for each applied signal level, using the TRMS voltmeter (Hi Z Input). Gain in DB is automatically calculated for each applied input using the following equation.

$$GAIN(DB) = 20 \text{ LOG } (OPT/VIN) + (MATCHIN + MATCHOT)$$

where OPT = Measured output voltage in millivolts RMS

VIN = Applied input in millivolts RMS

MATCHIN = Insertion loss in DB of the input matching network

MATCHOT = Insertion loss in DB of the output matching network

The measured gain is compared with the upper and lower limits for the test FAIL/PASS decision.

2.2.2 Freq. Range 60 KHZ - 100 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-4). Matching networks of known insertion loss as indicated in the ID diagram, may be required in the ID design. The parameters entered to AGEN are the same as above except the input voltage to UUT is entered in DBM. (RFB is used as the signal source.)

At the execution of the UUT test program, UUT output is measured for each applied signal level, using the TRMS voltmeter (50Ω Zin). The measured values are automatically converted into DBM using the following equation.

$$MDBO = 20 \text{ LOG } (OPT/224)$$

where MDBO = Output in DBM

OPT = Measured output in millvolts RMS

Gain is then calculated for each input level automatically using the

following equation.

GAIN(DB) = MDBO + MATCHOT + MATCHIN - DBIN

where MDBO = Output in DBM, calculated previously

MATCHOT = Insertion loss in DB of the output matching network

MATCHIN = Insertion loss in DB of the input matching network

DBIN = Applied signal in DBM from RFB to I D as UUT input

The measured gain is compared with the upper and lower limits for the test FAIL/PASS decision.

2.3 OSCILLATOR FREQUENCY STABILITY TEST

The frequency stability of an oscillator is the ability to generate a frequency which is precisely controlled within specified limits. The frequency at the UUT output is measured at constant intervals to test that the drift in frequency does not exceed the specified tolerance.

2.3.1 Freq. Range 2 HZ - 1 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-5). The user will then enter the following parameters to the AGEN to generate the UUT test program.

- DC power input
- Measurement time for the stability test
  (Measurements will be made every 5 seconds in the length of time selected by the user)
- Nominal frequency at UUT output
- Permissible deviation in the frequency output
  (AGEN will calculate the upper and lower limits of the frequency measurements)
- Maximum RMS volts at UUT output
- Threshold level for the frequency counter input
- Frequency range (2 HZ to 1 MHZ or 60 KHZ to 100 MHZ)

At the execution of the UUT test program, the frequency at the UUT output is measured every 5 seconds by the frequency counter (Hi Z Input). The measured values are compared with the upper and lower limits for the test PASS/FAIL decision.

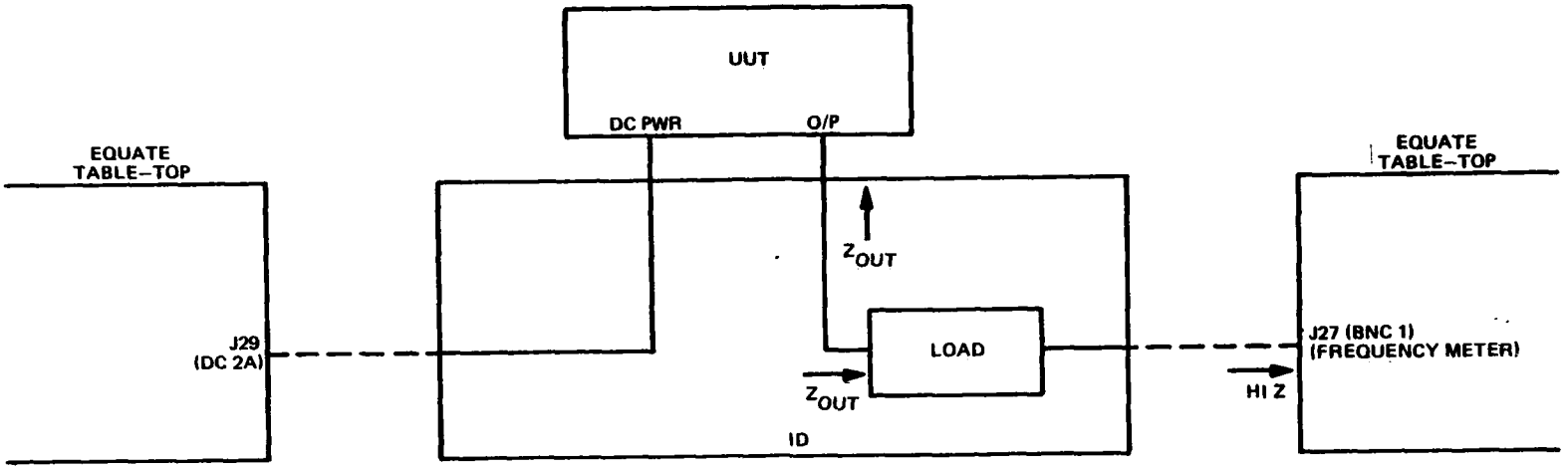
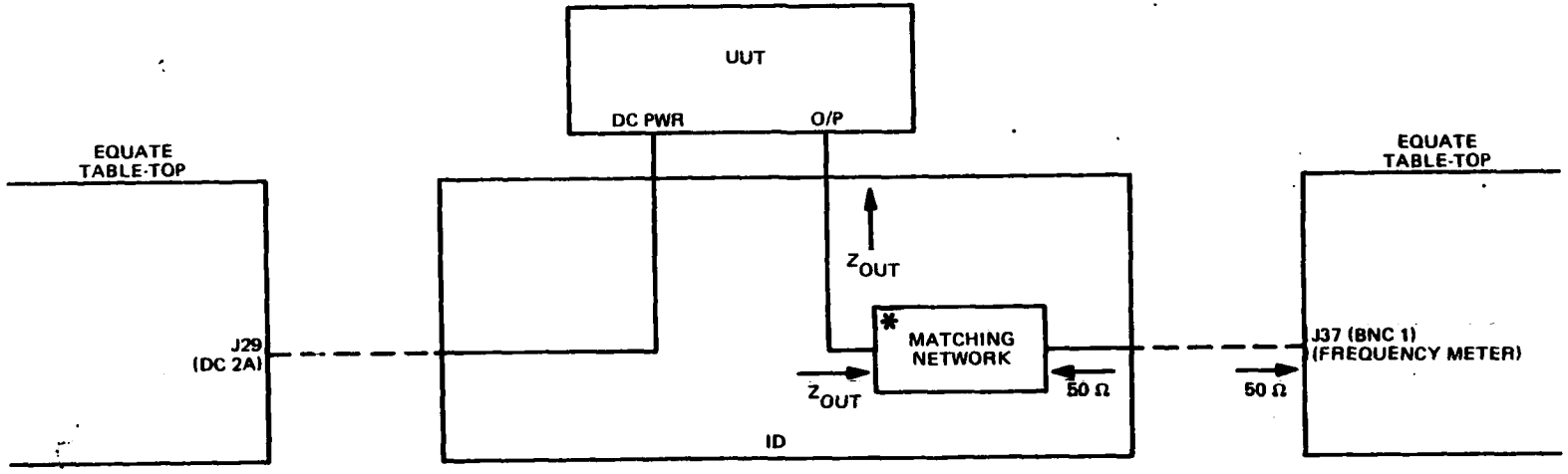


Figure 2-5. ID Diagram: Oscillator Frequency Stability Test - Frequency 2 Hz - 1 MHz



*MATCHING NETWORK IS REQUIRED IF UUT OUTPUT IS NOT MATCHED WITH 50 Ω LOAD.

Figure 2-6. ID Diagram: Oscillator Frequency Stability Test - Frequency 60 kHz - 100 MHz

2.3.2 Freq. Range 60 KHZ - 100 MHZ

The user designs the ID according to the ID diagram (fig. 2-6). The parameters entered to AGEN and the measurement technique is the same as above except the 50 OHM Zin frequency counter is used as the measurement device.

2.4 OSCILLATOR AMPLITUDE STABILITY TEST

The output of the oscillator is measured as being at a particular amplitude within a specified tolerance. The stability is the ability of the oscillator to maintain its output within the limits over a period of time. The amplitude at the UUT output is measured at constant intervals to test that the drift in frequency does not exceed the specified tolerance.

2.4.1 Freq. Range 2 HZ - 1 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-7). The user will then enter the following parameters to the AGEN to generate the UUT test program.

- DC power input
- Measurement time length for the stability test
  (Measurement will be made every 5 seconds in the time selected by the user)
- Maximum frequency at UUT output
- Nominal output amplitude
- Output amplitude deviation
  (AGEN will calculate the upper and lower limits of the amplitude measurements)
- Frequency range (2 HZ to 1 MHZ or 60 KHZ to 100 MHZ)

At the execution of the UUT test program, the amplitude at the UUT output is measured every 5 seconds by the TRMS voltmeter (Hi Z input). The measured values are compared with the upper and lower limits for the test FAIL/PASS decision.

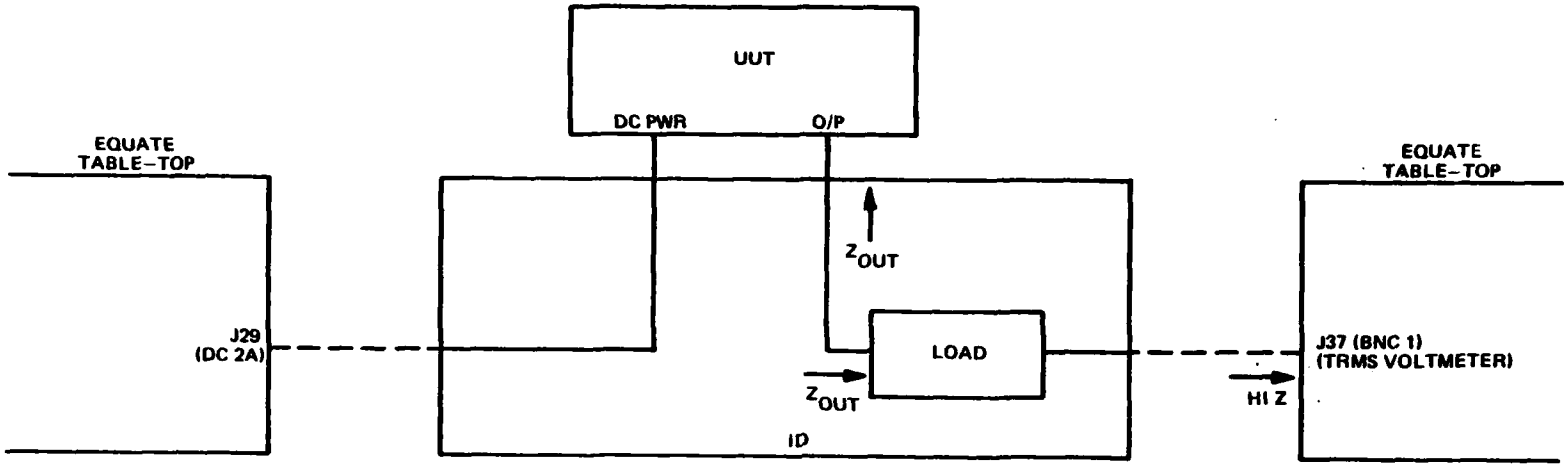


Figure 2-7. ID Diagram: Oscillator Amplitude Stability Test - Frequency 2 Hz - 1 MHz

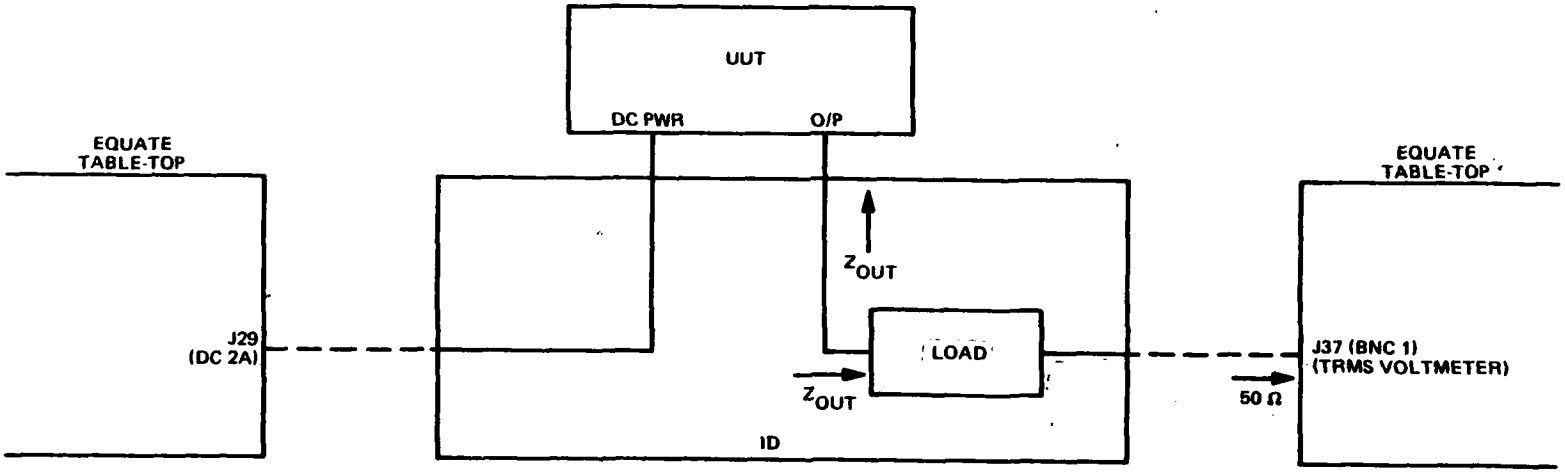


Figure 2-8. ID Diagram: Oscillator Amplitude Stability Test - Frequency 60 kHz - 100 MHz

2.4.2 Freq. Range 60 KHZ - 100 MHZ

The user designs the ID according to the ID diagram (fig. 2-8). The parameters entered to AGEN and the measurement technique is the same as in 2.4.1 except TRMS voltmeter (50Ω Z in) is used as the measurement device.

2.5 POWER SUPPLY REGULATION TEST

Regulation is a measure of how well the output voltage remains constant as related to load or line variations. AC or DC power is applied to the UUT input and the output is measured in the two conditions:

(1) Full Load
(2) Input voltage varied between the upper and lower limits (DC input only).

The AGEN user designs the ID according to the ID diagram (fig. 2-9). The user will then enter the following parameters to the AGEN to generate the UUT test program.

- AC or DC input
  (115 V AC will be applied if AC input is selected)
- Nominal DC voltage applied to UUT input
- Permissible deviation in the applied DC voltage
  (AGEN will compute the maximum and minimum DC voltage for the UUT input)
- Number of UUT outputs (NUM)
- Nominal DC voltage at each output
- Permissible deviation at each output,
  AGEN will compute the upper and lower limits for each output (VOUL 1 - VOUL 6, VOLL 1 - VOLL 6)

At the execution of the UUT test program, AC or DC voltages are applied to UUT input and the output voltage is measured after the maximum load has been applied. The input regulation test is performed by measuring the UUT output voltage when minimum and maximum DC voltages are applied. If the required input to UUT is AC then the line regulation test is not performed because 115V AC from EQUATE cannot be varied. The measured DC voltage from each output is compared with the upper and lower limits for the test FAIL/PASS decision.

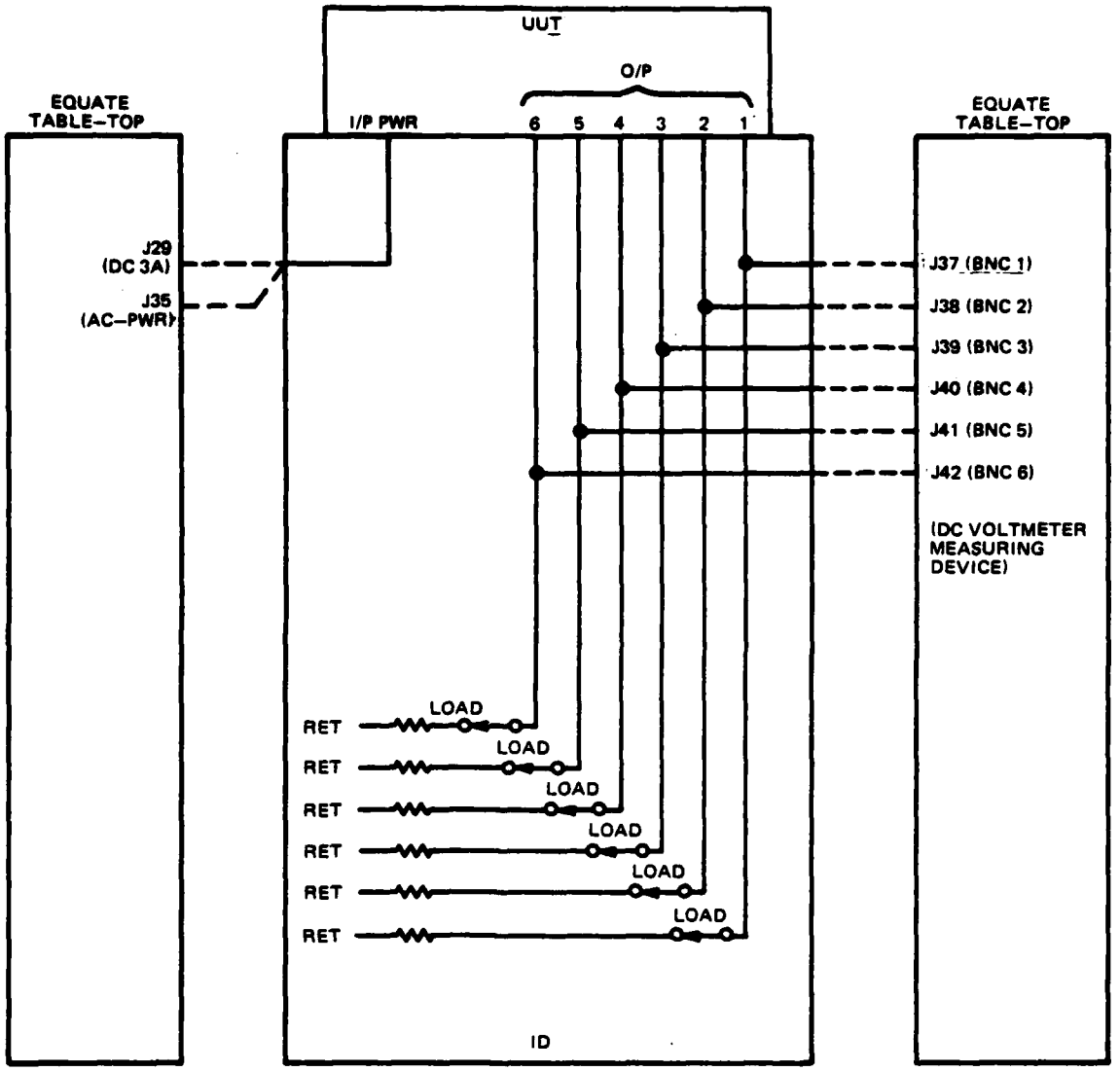


Figure 2-9. ID Diagram: Power Supply Regulation Test

2.6 POWER SUPPLY RIPPLE TEST

Ripple is the amount of the AC voltage that is riding on the DC output. In an operating power supply, this will be a very small percentage of the output. The AC component at the UUT output is measured by the AC-coupled TRMS voltmeter.

The AGEN user designs the ID according to the ID diagram (fig.2-10). The user will then enter the following parameters to the AGEN to generate the UUT test program.

- AC or DC input
  115V AC will be applied if AC input is selected
- Nominal DC voltage applied to UUT input
- Number of UUT outputs
- Nominal DC voltage at each output
- Maximum ripple voltage at each output

At the execution of the UUT test program, AC or DC voltage is applied to the UUT input and the ripple is measured in volts RMS at each output. The measured values are compared with the maximum ripple voltage at each output for the test FAIL/PASS decision.

2.7 POWER SUPPLY OVERCURRENT TEST

Overcurrent protection is the ability of the power supply to automatically reduce its output voltage to a low voltage if the output current exceeds its maximum current by a specified amount. The overcurrent voltage is measured after the overcurrent load has been applied to the UUT output.

The AGEN user designs the ID according to the ID diagram (fig. 2-11). The user will then enter the following parameters to the AGEN to generate the UUT test program.

- AC or DC input
  (115V AC will be applied if AC input is selected)
- Nominal DC voltage applied to UUT input.
- Number of UUT outputs
- Nominal DC voltage at each output
- Maximum overcurrent voltage at each output.

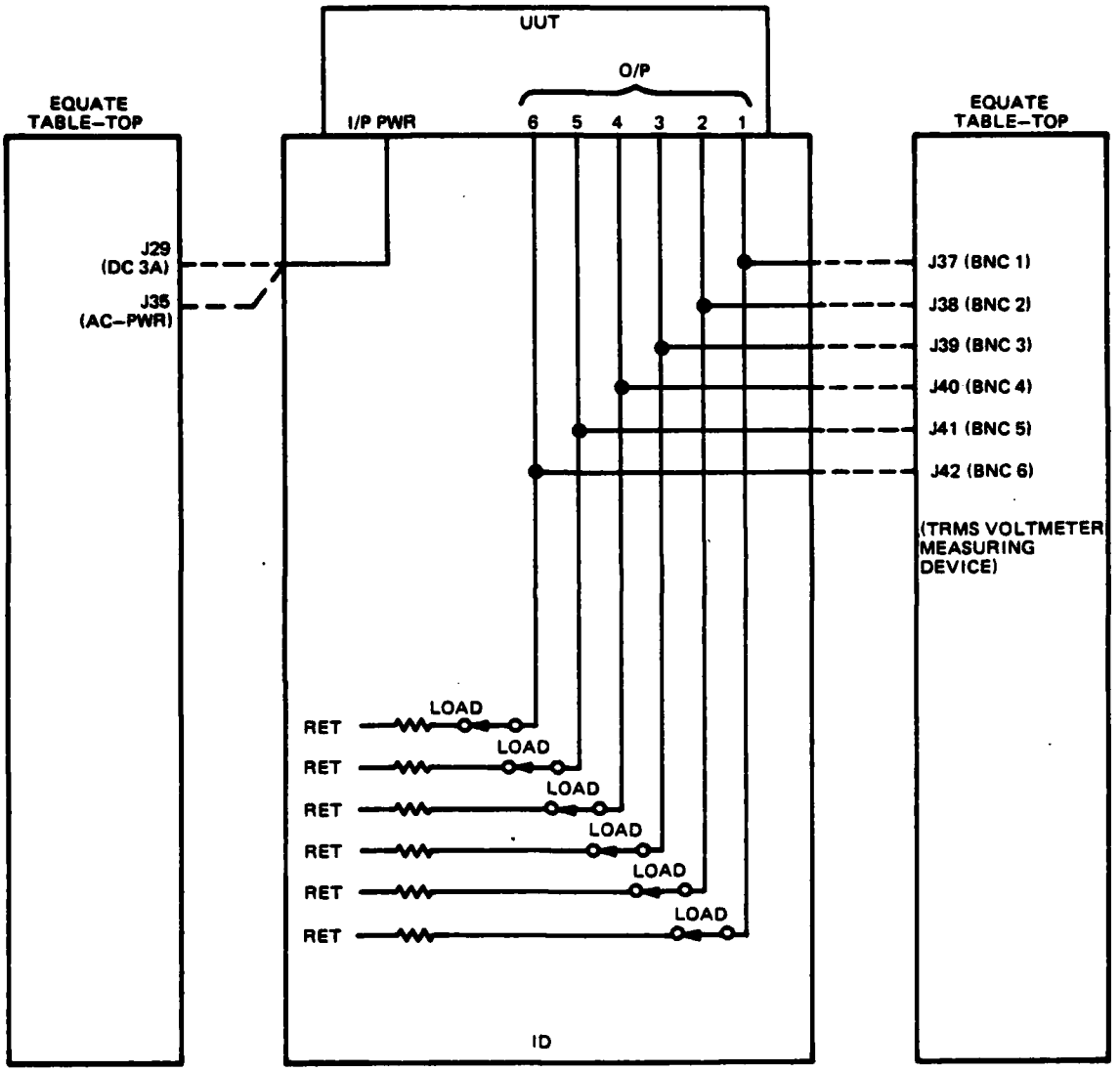


Figure 2-10. ID Diagram: Power Supply Ripple Test

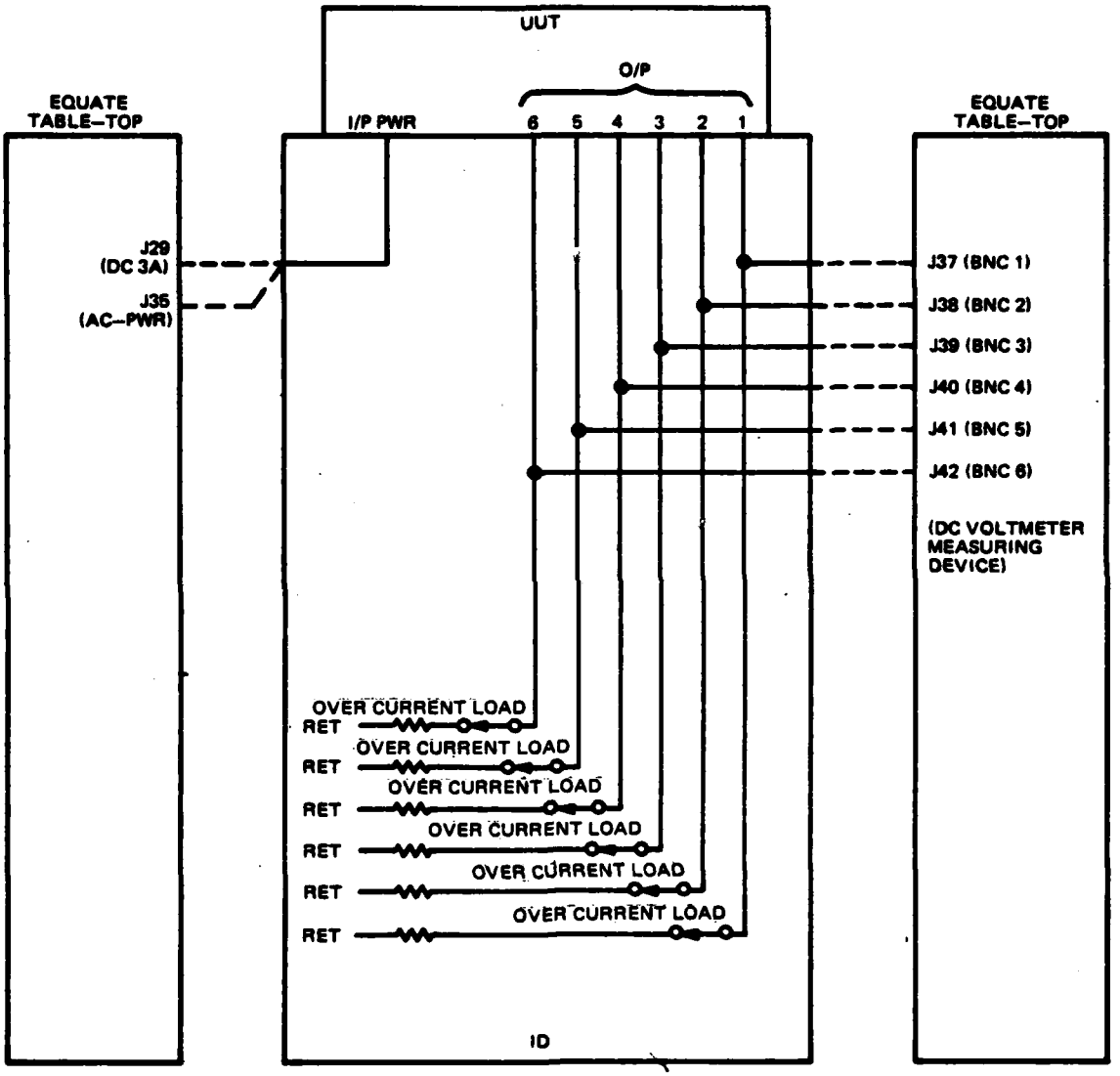


Figure 2-11. ID Diagram: Power Supply Over-Current Test

At the execution of the UUT test program, AC or DC voltage is applied to the UUT input and the UUT output voltage is measured at each output after the overcurrent loads have been applied. The measured values are compared with the maximum overcurrent voltage at each output for the test FAIL/PASS decision.

2.8 MIXER ISOLATION TEST

Mixer's local oscillator (LO) to IF Port isolation is measured by calculating the ratio in DB of the LO signal present at the IF output to the LO signal at the mixer input. The mixer IF output is then passed through a bandpass filter which rejects all the frequencies except the LO frequency component present at the IF output. The characteristic of the bandpass filter used at the IF output must be such that it is able to reject all the frequencies, except the LO component.

The AGEN user designs the ID according to the ID diagram (fig 2-12). Matching networks of known insertion loss, as indicated in the ID diagram, may be required in the ID design. The user can then enter the following parameters to the AGEN to obtain the UUT test program.

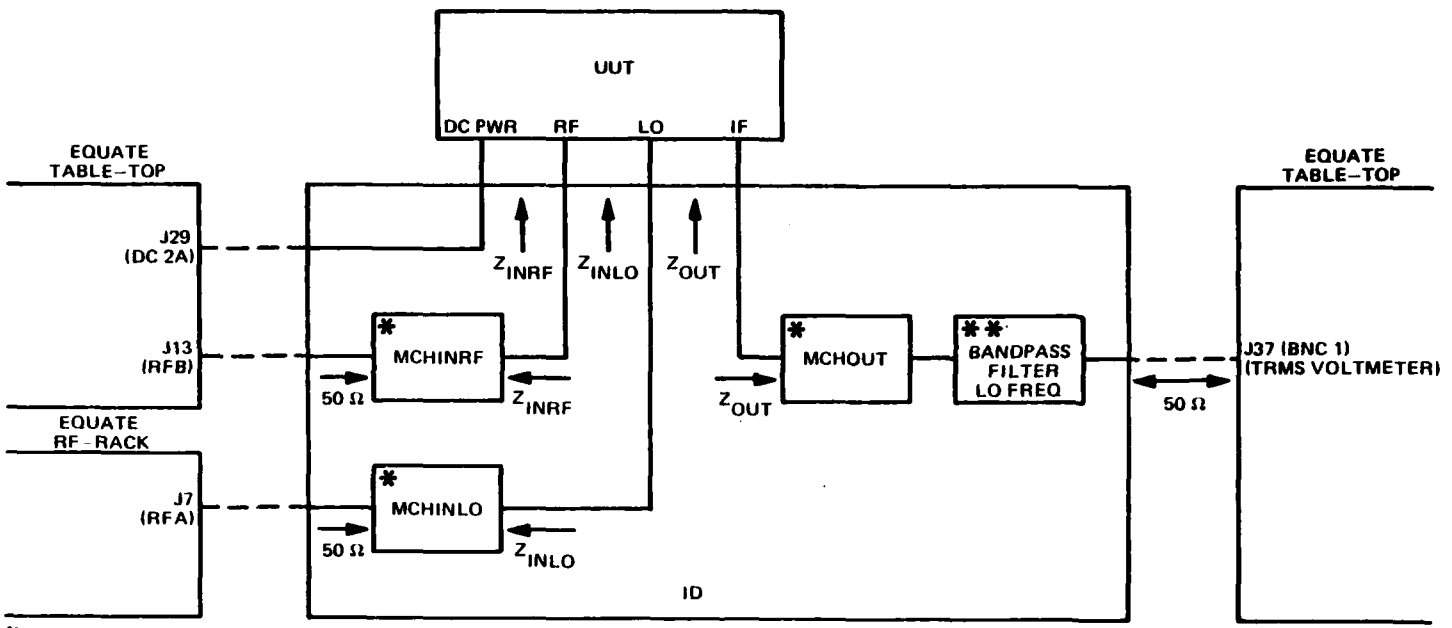
- Power Supply (VDC)
- Signal amplitude in DBM from RFB to ID for UUT RF input (PRF)
- Signal amplitude in DBM from RFA to ID for UUT LO input (PLO)
- Nominal frequency at RF input (RF)
- Nominal frequency at LO input (LO)
- Insertion loss in DB of the matching network at UUT RF input (MCHINRF)
- Insertion loss in DB of the matching network at UUT LO input (MCHINLO)
- Insertion loss in DB of the matching network at UUT output (MCHOUT)
- Minimum isolation in DB between LO and IF ports (ISOLL)

During the execution of UUT test program, the LO frequency component at IF output is measured in millivolts RMS. Measured voltage is automatically converted into DBM using the following equation:

$$MDBLOIF = 20 \log (MVLOIF/224)$$

where MDBLOIF = Measured voltage in DBM

MVLOIF = Measured LO component at IF output in millivolts RMS



*MATCHING NETWORKS OF KNOWN INSERTION LOSS ARE REQUIRED IF UUT INPUTS AND OUTPUT ARE NOT MATCHED WITH 50 OHM SOURCE AND LOAD.

**THE BANDPASS FILTER SHOULD REJECT ALL FREQUENCIES EXCEPT LO FREQUENCY.

Figure 2-12. ID Diagram: Mixer Isolation Test (LO-IF Port) - Frequency 60 kHz - 100 MHz

Isolation in DB is then calculated using the following equation automatically:

MISO = PLO - (MCHINLO + MCHOUT - MDBLOIF)

where MISO = Measured isolation in DB

PLO = Signal amplitude in DBM from RFA to ID for UUT LO input.

MCHINLO = Insertion loss in DB of the matching network at UUT LO input

MCHINRF = Insertion loss in DB of the matching network at UUT RF input

MCHOUT = Insertion loss in DB of the matching network at UUT output

The measured isolation value is compared with the minimum isolation value for the test FAIL/PASS decision.

2.9 MIXER FREQUENCY RESPONSE TEST

The Mixer frequency response test is a confidence check that an IF above a threshold level does exist at the UUT output. The IF is then compared with the nominal IF entered by the user. Five sets of RF and LO frequencies are used to ensure the UUT operation is in its entire frequency range.

The AGEN user designs the ID according to the ID diagram (fig. 2-13). Matching networks, as indicated in the ID diagram, may be required in the ID design. The user will then enter the following parameters to the AGEN to generate the UUT test program.

- Power Supply (VDC)
- Signal amplitude in DBM from RFB to ID as UUT RF input (PRF)
- Signal amplitude in DBM from RFA to ID as UUT LO input (PLO)
- Threshold level in millivolts at the measuring device (VTHRSH)
- Nominal intermediate frequency at UUT output (IF)
- Five frequencies for RF input (RF1 to RF5) (corresponding LO frequencies are calculated in AGEN).

During the execution of the UUT test program, the frequency at the IF output is measured for each set of RF-LO frequencies. The measured value is compared within $\pm$0.1 KHZ of the Nominal IF for the test FAIL/PASS decision.

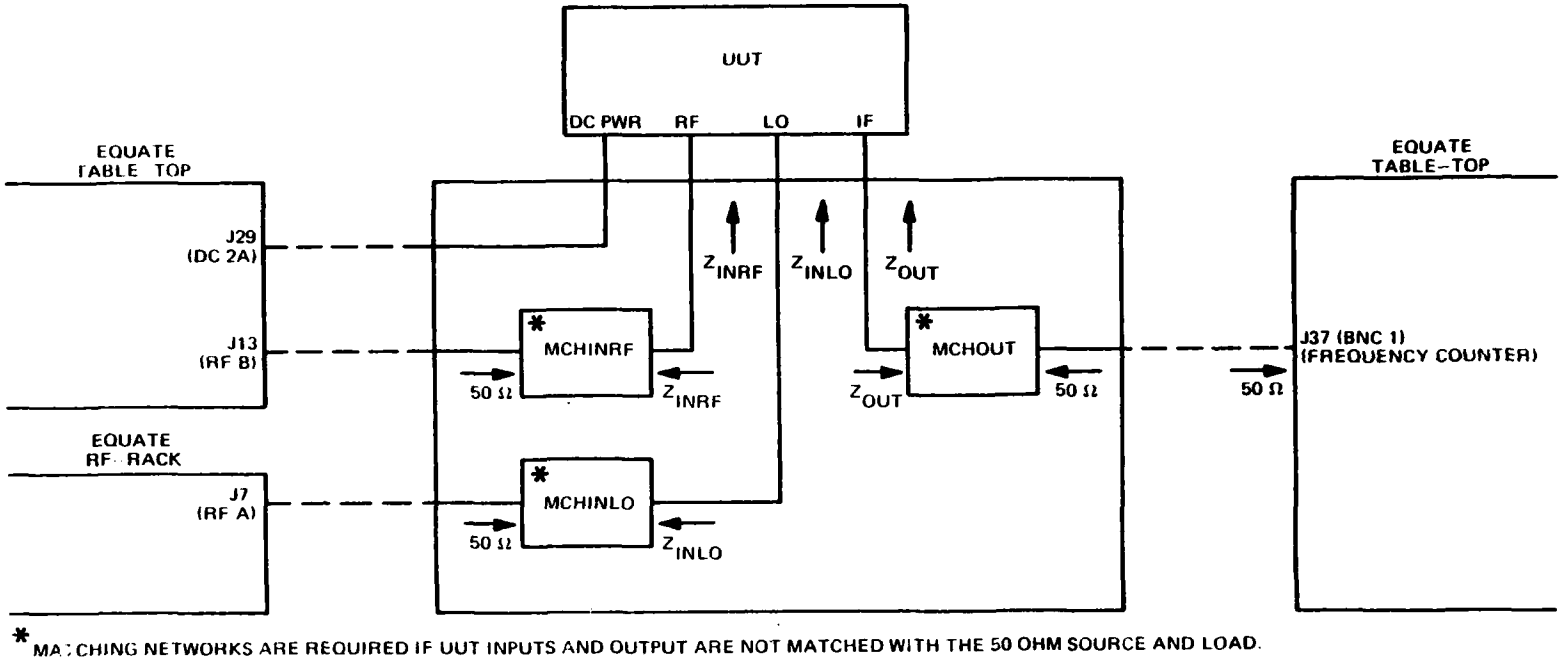


Figure 2-13. ID Diagram: Mixer Frequency Response Test - Frequency 60 kHz - 100 MHz

2.10 MIXER CONVERSION LOSS TEST

Conversion loss is measured by calculating the ratio in DB of the signal amplitude at IF output and the RF input. Five sets of RF and LO frequencies are used to measure the conversion loss in the entire frequency range of the UUT.

The AGEN user designs the ID according to the ID diagram (fig.2-14). Matching networks of known insertion loss, as indicated in the ID diagram, may be required in the ID design. The user will then enter the following parameters to the AGEN to generate the UUT test program.

- Power Supply (VDC)
- Signal amplitude in DBM from RFB to ID as UUT RF input (PRF)
- Signal amplitude in DBM from RFA to ID as UUT LO input (PLO)
- Nominal frequency at IF output (IF)
- Five frequencies for RF input (RF 1 to RF 5, the corresponding LO frequencies are calculated in AGEN)
- Insertion loss of the matching network at UUT RF input (MCHINRF)
- Insertion loss of the matching network at UUT LO input (MCHINLO)
- Insertion loss of the matching network at UUT output (MCHOUT)
- Maximum conversion loss value (LOSSUL)

During the execution of UUT test program, signal amplitude at IF output is measured in millvolts RMS for each set of RF-LO frequencies. Each measured output is automatically converted into DBM using the following equations:

MDBIF = 20 LOG (MVIF/224)

where MDBIF = Measured voltage in DBM

MVIF = Measured IF in millivolts RMS

Conversion loss is then calculated automatically for each set of applied LO-RF frequencies, using the following equation.

MLOSS = PRF-(MCHINRF + MCHOUT + MDBIF)

where MLOSS = Conversion loss in DB

PRF = Signal level in DBM from RFB to ID as UUT RF input

MCHINRF = Insertion loss in DB of the matching network for UUT RF input

MCHOUT = Insertion loss in DB of the matching network at UUT output

MDBIF = IF output in DBM, calculated above.

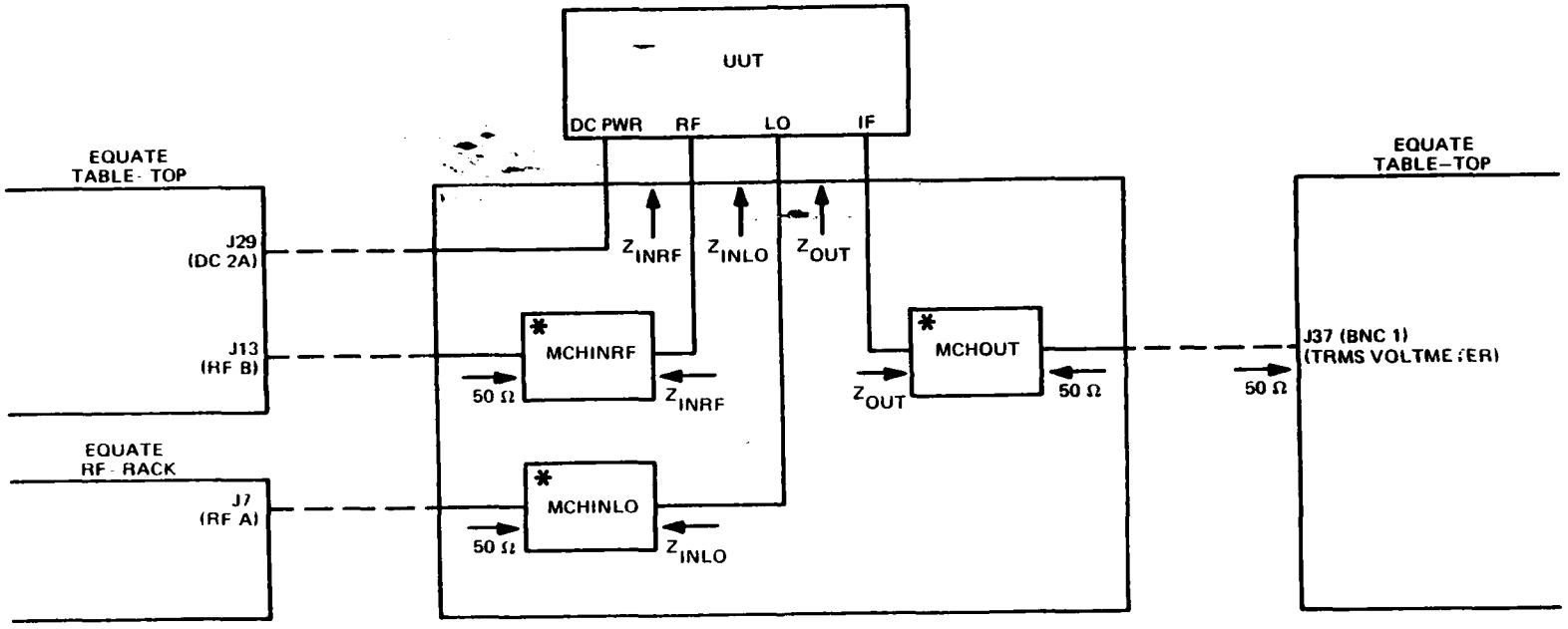


Figure 2-14. ID Diagram: Mixer Conversion Loss Test - Frequency 60 kHz - 100 MHz

The measured conversion loss value is compared with the maximum conversion loss value for the test FAIL/PASS decision.

2.11 FILTER INSERTION LOSS TEST

Filter insertion loss is the signal loss in DB when the frequency of the applied signal is within the passband. The UUT's in AGEN are divided into two groups according to their frequency range.

2.11.1 Freq. Range 2 HZ - 1 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-15). Matching networks of known insertion loss, as indicated in the ID diagram, may be required in the ID design. The user will then enter the following parameters to generate the test program.

- DC power input
- Frequency at which insertion loss is to be measured
- Signal amplitude in millivolts RMS from waveform generator to ID as UUT input
- Frequency range choice
- Insertion loss in DB of the input matching network
- Insertion loss in DB of the output matching network
- Maximum insertion loss in DB at the selected frequency.

At the execution of the test program, UUT output is measured in millivolts RMS. Insertion loss in DB is automatically calculated by the following equation.

INS LOSS (DB) = 20 LOG (VIN/MVOUT) - (MATCHIN + MATCHOT)

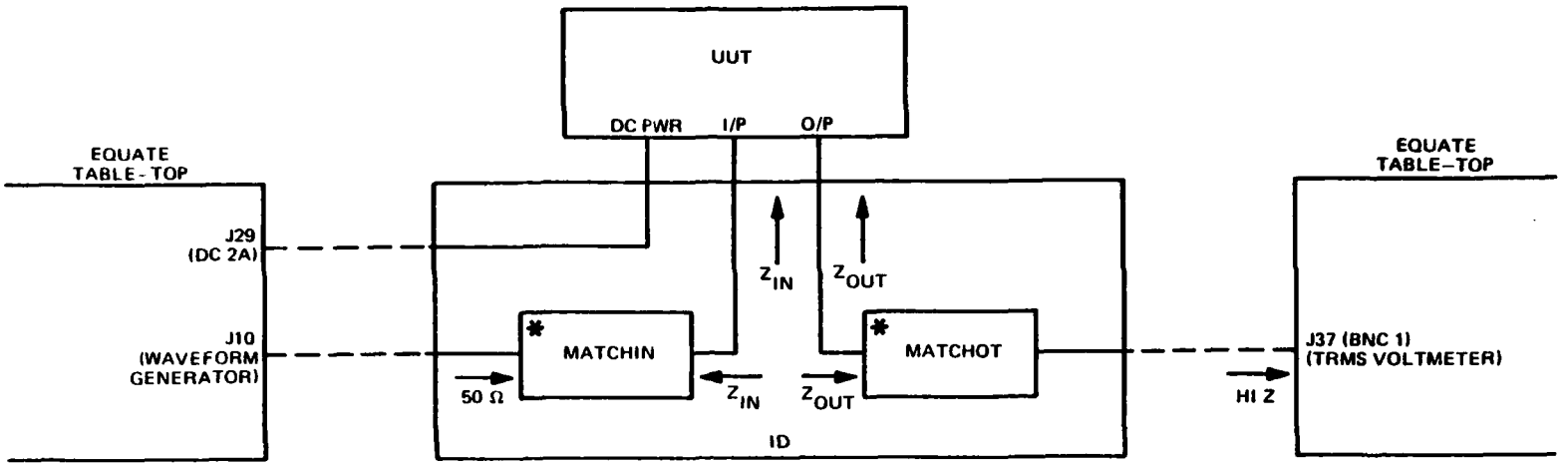
where VIN = Signal amplitude in millivolts RMS from waveform generator to ID for UUT input

MVOUT = Measured output in millivolts RMS

MATCHIN = Insertion loss in DB of the input matching network

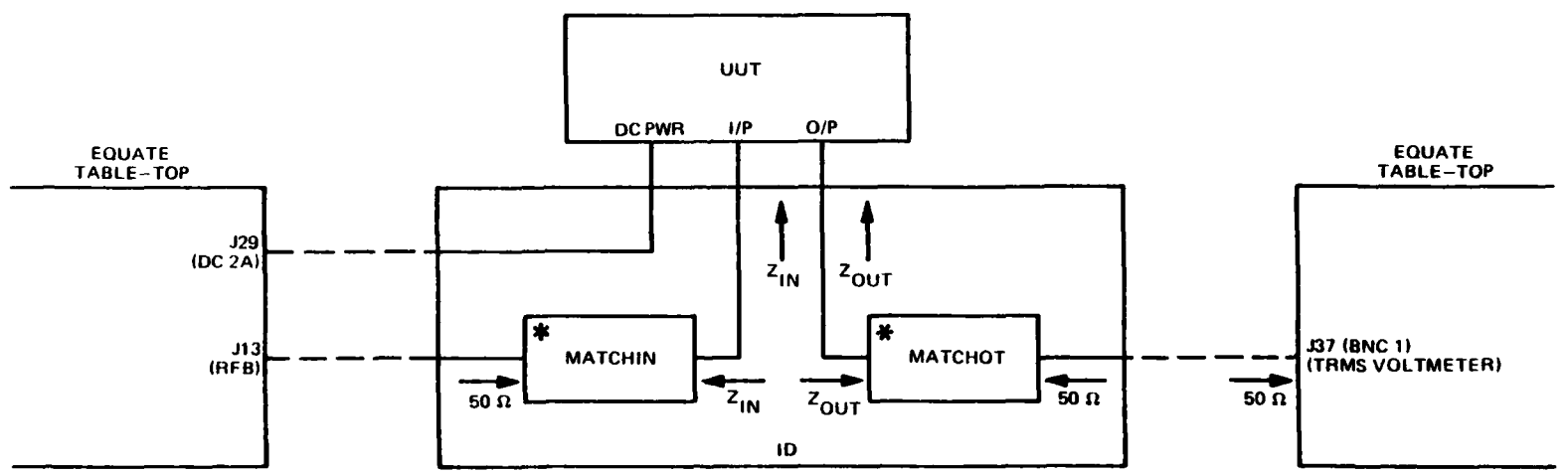
MATCHOT = Insertion loss in DB of the output matching network

The measured insertion loss is compared with the maximum insertion loss value for the test PASS/FAIL decision.



*MATCHING NETWORKS OF KNOWN INSERTION LOSS ARE REQUIRED IF UUT INPUT AND OUTPUT ARE NOT MATCHED WITH THE 50 OHM SOURCE AND HI Z LOAD.

Figure 2-15. ID Diagram: Filter Insertion Loss Test - Frequency 2 Hz - 1 MHz



*MATCHING NETWORKS OF KNOWN INSERTION LOSS ARE REQUIRED IF UUT INPUT AND OUTPUT ARE NOT MATCHED WITH 50 OHM SOURCE AND LOAD

Figure 2-16. ID Diagram: Filter Insertion Loss Test - Frequency 60 kHz - 100 MHz

2.11.2 Freq. Range 60 KHZ - 100 MHZ

The user designs the ID according to the ID diagram (fig.2-16). Matching networks of known insertion loss may be required in the ID diagram. The parameters entered to AGEN are the same as in 2.11.1 except signal amplitude to ID as UUT input is entered in DBM (RFD is used as the frequency source).

At the execution of the test program,UUT output is measured by the TRMS voltmeter (Hi Z Input). The measured output is converted into DBM using the following equation:

MDBO = 20 LOG (MVOUT/224)

where MDBO = UUT output in DBM

MVOUT = Measured output in millivolts RMS

Insertion loss in DB is then calculated automatically using the following equation:

INS LOSS (DB) = DBIN-(MDBO + MATCHOT + MATCHIN)

where DBIN = Signal amplitude in DBM from RFB to ID for UUT input

MDBO = UUT output in DBM, calculated above.

MATCHOT = Insertion loss in DB of the output matching network

MATCHIN = Insertion loss in DB of the input matching network

The measured insertion loss value is compared with the maximum value for the test FAIL/PASS decision.

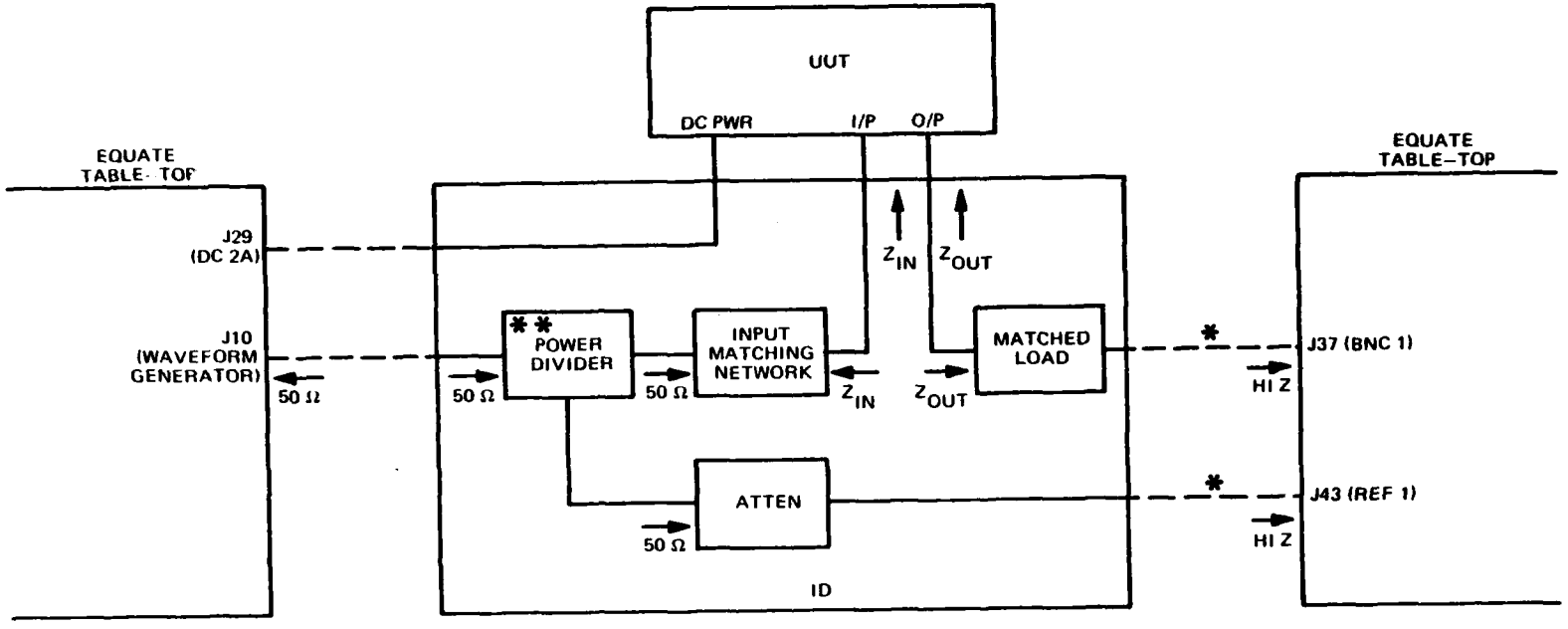
2.12 FILTER PHASE MEASUREMENT TEST

The phase response of a filter is a measure of the variation of phase shift between UUT input and output when the frequency of the applied signal is varied. The UUT's in AGEN are divided into two groups according to their frequency range.

2.12.1 Freq. Range 2 HZ - 1 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-17). The user will then enter the following parameters to the AGEN to generate the UUT test program:

- DC power input
- Five frequencies at which phase measurement is required



* THE LENGTHS OF THE CABLES FOR THE TWO RF PATHS SHOULD BE KEPT EQUAL. (PHASE SHIFT AT 10 MHz = 12°/METER.)

** FREQUENCY RANGE 50 kHz – 10 MHz, e.g. PD-20-10.

Figure 2-17. ID Diagram: Filter Phase Measurement (2 Hz - 1 MHz)

- Nominal phase shift at each test frequency
- Permissible deviation in phase shift values (AGEN will compute the upper and lower limits of the phase shift measurements)
- Signal amplitude from waveform generator to ID as UUT input
- Frequency range choice

At the execution of the test program, signal from waveform generator is applied to power divider in the ID. One output from power divider is applied to phase meter reference input and the other output is applied to UUT input. Phase angle is measured for each frequency by the phase meter (Hi Z Input). The measured values are compared with the upper and lower limits for the test FAIL/PASS decision.

2.12.2 Freq. Range 60 KHZ - 10 MHZ

The frequency range is limited to 10 MHZ due to the phase measurement capability of the EQUATE station. The user designs the ID according to ID diagram (fig 2-18). The parameters entered to AGEN are same as above except the signal amplitude to ID for UUT input is entered in DBM (RFB is used as the signal source).

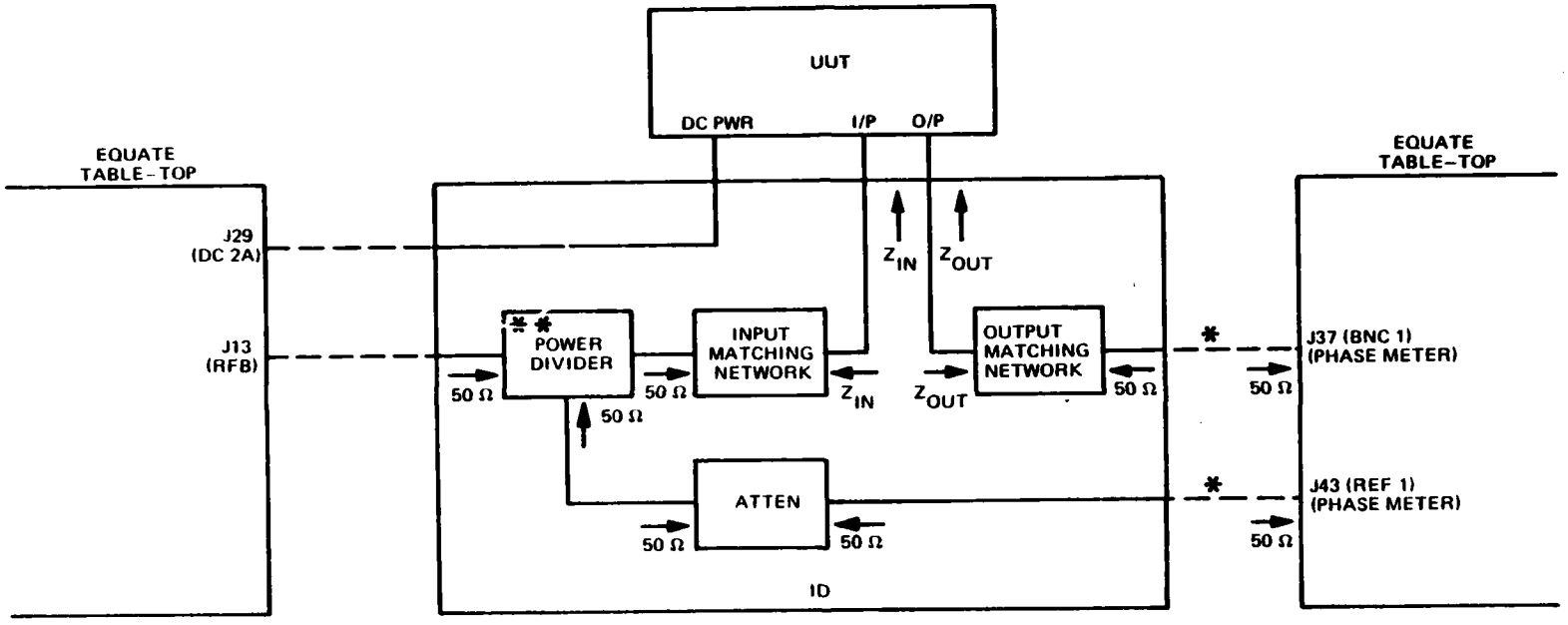
At the execution of the test program, phase angle is measured for each frequency input by the phase meter (50Ω Zin). The measured values are compared with the upper and lower limits for the test FAIL/PASS decision.

2.13 FILTER INPUT IMPEDANCE TEST

Input impedance is the impedance seen by looking into the input port of the Filter considering the Filter as a two-port network. The Filter is terminated with a load that matches its output impedance. The UUT's in AGEN are divided into two groups according to their frequency range.

2.13.1 Freq. Range 2 HZ - 1 MHZ

Input impedance is measured by measuring the voltage drop across a known resistance at the UUT input. The resistance value is selected in the ID design. The AGEN user designs the ID according to the ID diagram (fig 2-19). Matching network as indicated in the ID diagram may be required in the ID design.



* THE LENGTHS OF THE CABLES FOR THE TWO RF PATHS SHOULD BE KEPT EQUAL. (PHASE SHIFT AT 10 MHz = 12°/METER.)

** FREQUENCY RANGE 50 kHz – 10 MHz, e.g. PD-20-10.

Figure 2-18. ID Diagram: Filter Phase Measurement (60 kHz - 10 MHz)

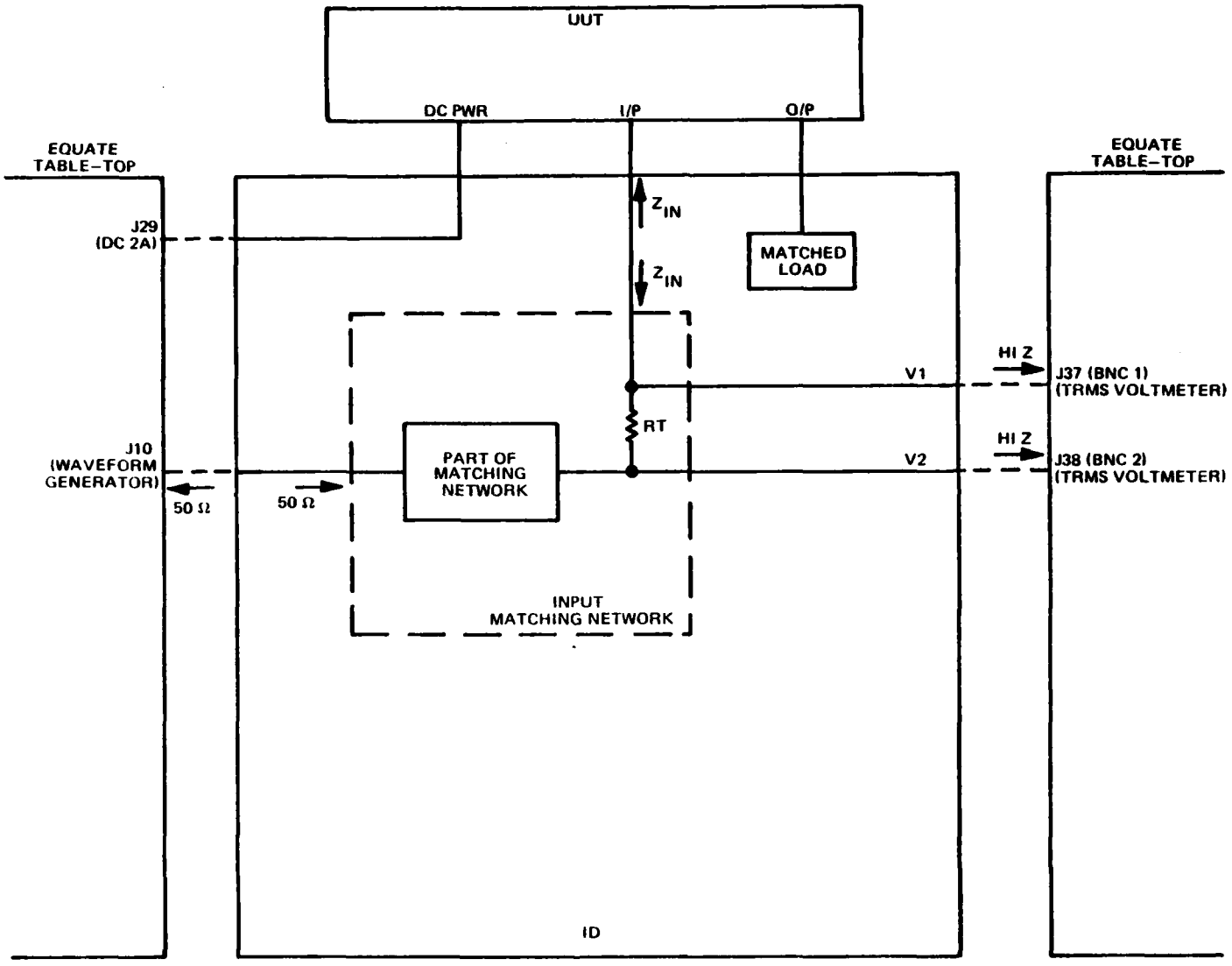


Figure 2-19. ID Diagram: Filter Input Impedance Measurement (2 Hz - 1 MHz)

The AGEN user then enters the following parameters into AGEN to generate the UUT test program:

- DC power input
- Frequency range choice
- Signal amplitude from waveform generator to ID as UUT input
- Frequency at which input impedance is measured
- Input impedance nominal value in ohms
- Permissible deviation in input impedance (AGEN will compute the upper and lower limit of the input impedance)
- Resistance in ohms of the input resistance in ID

At the execution of the UUT test program, voltages on both sides of the known resistor at the UUT input is measured in volts RMS. The absolute value of input impedance is automatically calculated using the following equation:

$$\text{Input Imp (ABS)} = VI \cdot RT/(V2-V1)$$

where RT = Resistance in ohms connected to UUT input

V1 = Measured voltage at the UUT side of the resistor RT.

V2 = Measured voltage at the other side of the resistor RT.

The measured input impedance is compared with the upper and lower limits of the input impedance values for the test PASS/FAIL decision.

2.13.2 Freq. Range 60 KHZ - 100 MHZ

The input impedance is measured by measuring the reflection coefficient at the UUT input. The AGEN user designs the ID according to the ID diagram (fig. 2-20). The parameters entered to the AGEN are essentially the same as above except input signal level to ID for UUT input is entered in DBM (RFB is used as the frequency source).

At the execution of the UUT test program, signal from RFB is applied to power divider (inside the ID) and then applied to two separate 50Ω tee connectors. Tee 1 is used to measure the reflection from UUT Input. Tee 2 is used to measure the reflection from a 50Ω load. DC voltmeter (Hi Z Input) is used to measure the detected voltages from the two 50Ω tees. The reflection coefficient is automatically calculated using the following equation:

$$RCOEF = VR/VIN - 1$$

where VR = Measured voltage in millivolts DC from

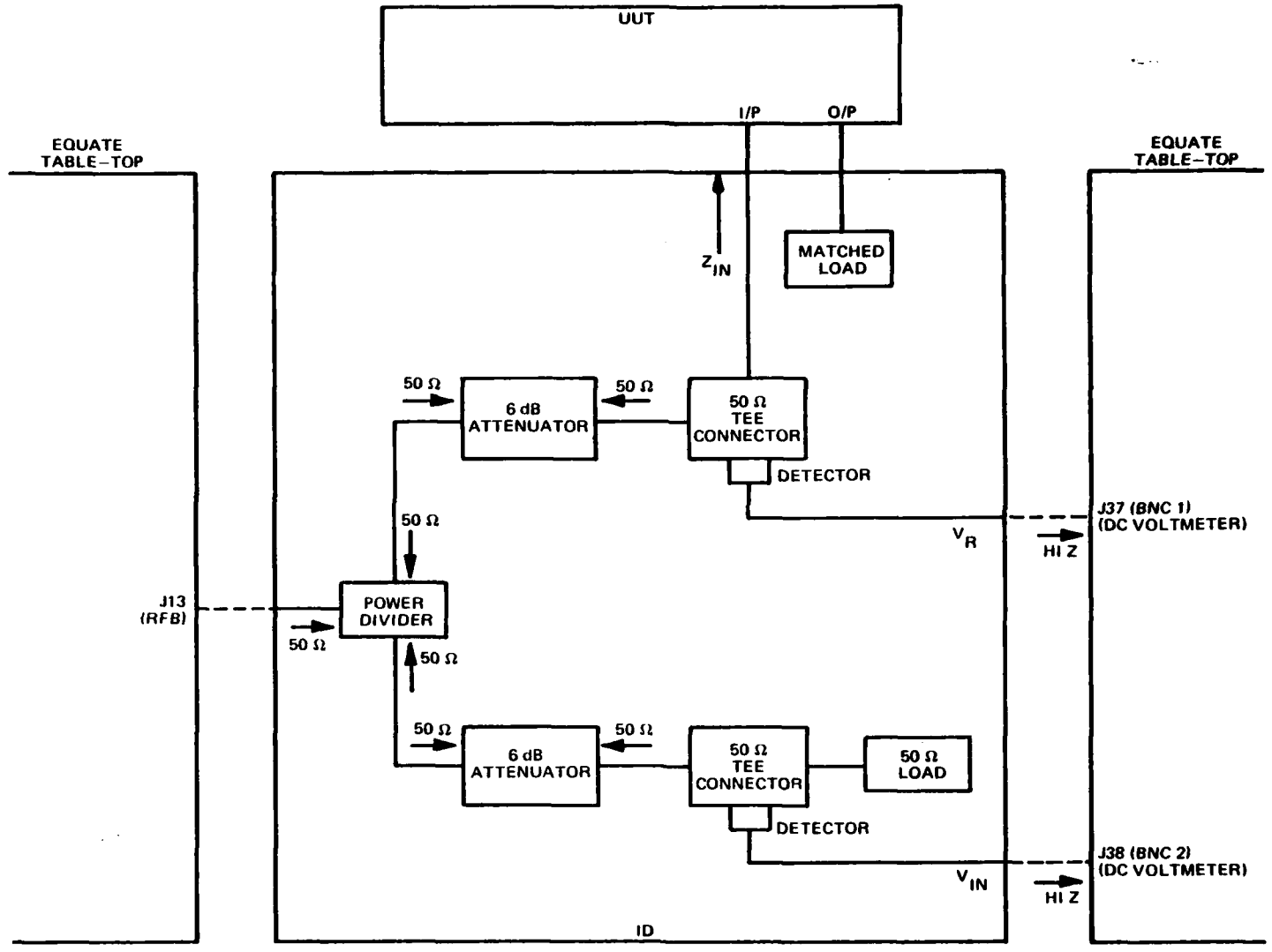


Figure 2-20. ID Diagram: Filter Input Impedance Measurement (60 kHz - 100 MHz)

the tee terminated by UUT input impedance.

VIN = Measured voltage in millivolts DC from the tee terminated by 50 ohms load.

RCOEF = Reflection Coefficient at UUT input

The absolute value of input impedance is calculated automatically by the following equations:

$$Z_{in}\ (ABS) = 50\ (1 + RCOEF)/(1-RCOEF)$$

$$Z_{in}\ (ABS) = 50\ (1 - RCOEF)/(1+RCOEF)$$

NOTE: First equation is true if $Z_{in}\ (ABS) > 50$ while second equation is true if $Z_{in}\ (ABS) > 50$.

Since ambiguity exists in the above calculation of input impedance, both values are displayed to the operator for manual FAIL/PASS decision.

2.14 FILTER OUTPUT IMPEDANCE TEST

Output impedance is the impedance seen by looking into the output port of the Filter considering the Filter as a two-port network. The Filter input is matched with a 50 ohm source impedance. The UUT's in AGEN are divided into two groups according to their frequency range.

2.14.1 Freq. Range 2 HZ - 1 MHZ

Output impedance is measured by measuring the voltage change when the UUT is terminated by two known resistor loads. The resistance values are selected in the ID design. The AGEN user designs the ID according to the ID diagram (fig. 2-21). Matching network as indicated in the ID design may be required in the ID design. The AGEN user then enters the following parameters into AGEN to generate the UUT test program.

- DC power input
- Frequency range choice
- Signal amplitude from waveform generator to ID as UUT input
- Frequency at which output impedance is measured
- Output impedance nominal value in ohms
- Permissible deviation in output impedance (AGEN will compute the upper and lower limit of the output impedance)
- Resistances in ohms of the two resistor loads (RT and RL) in the ID

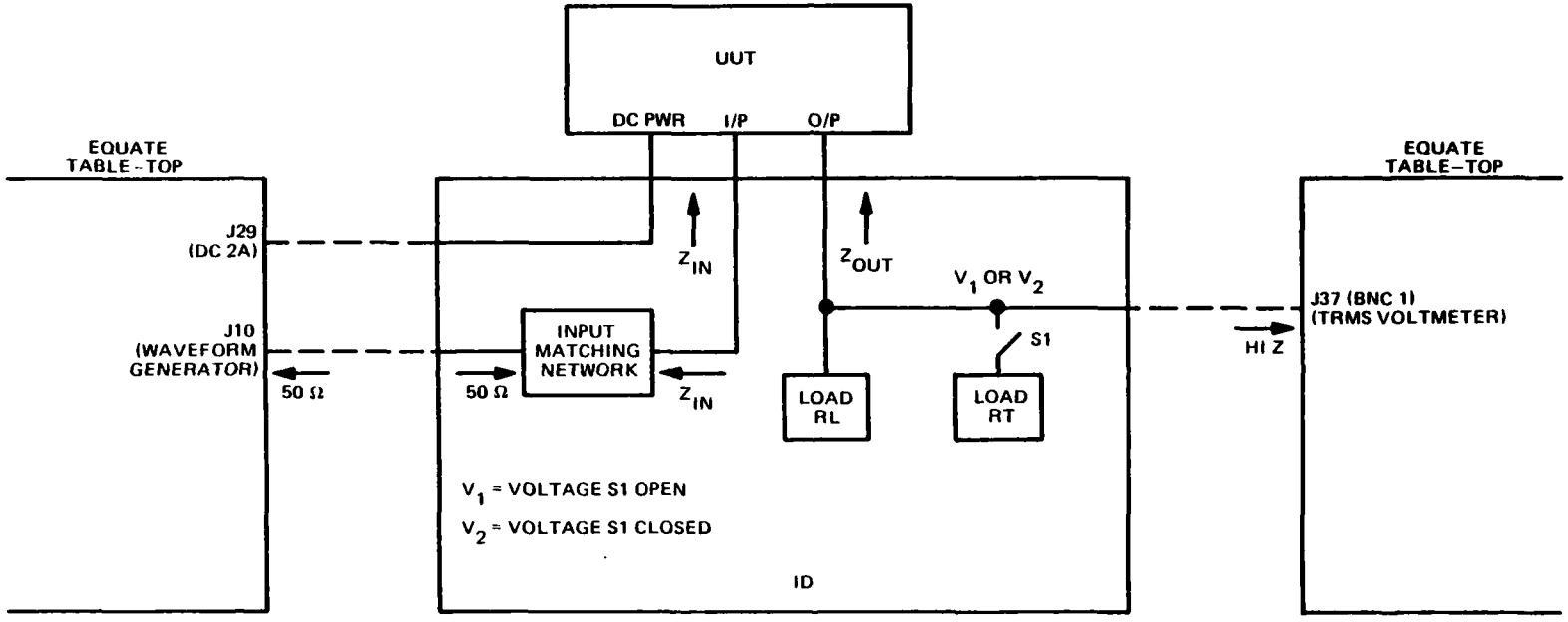
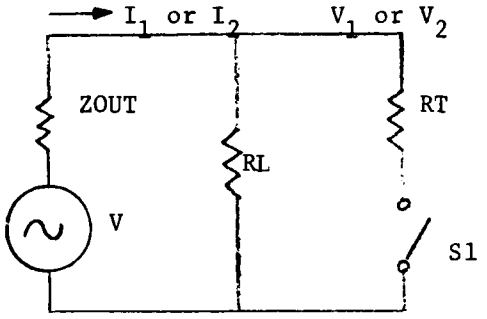


Figure 2-21. ID Diagram Filter Output Impedance Measurement (2 Hz - 1 MHz)

At the execution of the test program, the UUT output is measured in two conditions:

1. UUT output terminated by the known resistance RL
2. UUT output terminated by the parallel combination of known resistance RL and RT

NOTE: The equivalent circuit of the UUT with ID may be considered as follows:



V1 = RMS Voltage with Switch S1 OPEN

V2 = RMS Voltage with Switch S1 CLOSED

S1 OPEN

$$V = \frac{V1}{RL}(RL + ZOUT)$$

$$= V1 + \frac{V1 \cdot ZOUT}{RL} \qquad \text{(1)}$$

S1 CLOSED

$$V = V2 \frac{(RT + RL)}{R + RL} \qquad (ZOUT + \frac{RT\ RL}{RT + RL})$$

ASSUMING $R3 = \frac{RT \cdot RL}{RT+RL}$

$$V = ZOUT \cdot Z2 + V2 \qquad \text{(2)}$$

Solving equations (1) and (2) we get

$$ZOUT = \frac{R3RL\ (V1 - V2)}{V2R1-V1R3}$$

The absolute value of the output impedance is automatically calculated by the above equation. The measured value is compared with the upper and lower limits of the output impedance for the test FAIL/PASS decision.

2.14.2 Freq. Range 60 KHZ - 100 MHZ

The output impedance can be measured only if the UUT is reversable i.e., if UUT output can be used as the input. The measurement of output impedance in AGEN is actually measurement of input impedance when the UUT is reversed (output is used as input). The AGEN user designs the ID diagram according to the ID diagram (fig.2-22). The parameters entered into AGEN and the execution of the test program is therefore the same as the measurement of input impedance as in 2.13.2.

2.15 FILTER AMPLITUDE RESPONSE TEST

Filter amplitude response is the variation of insertion loss with frequencies. The loss should be a minimum value in the passband and a maximum value in the stopband. The current AGEN is limited to bandpass filters only. The UUT's in AGEN are divided into two groups according to their frequency range.

2.15.1 Freq. Range 2 HZ - 1 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-23). Matching networks of known insertion loss, as indicated in the ID diagram, may be required in the ID design. The user will then enter the following parameters to generate the test program.

- Frequency range choice
- DC power input
- Nine frequencies, three in lower stopband, three in passband and three in upper stopband.
- Signal amplitude from waveform generator to ID as UUT input.
- Maximum insertion loss in DB in the UUT passband.
- Minimum rejection in DB in the UUT stopband.
- Insertion loss in DB of the input matching network.
- Insertion loss in DB of the output matching network.

As an AGEN option, if 3 DB measurements are desired, then the user will be required to enter the following parameters in addition to the above parameters.

- Upper 3 DB point frequency
- Lower 3 DB point frequency

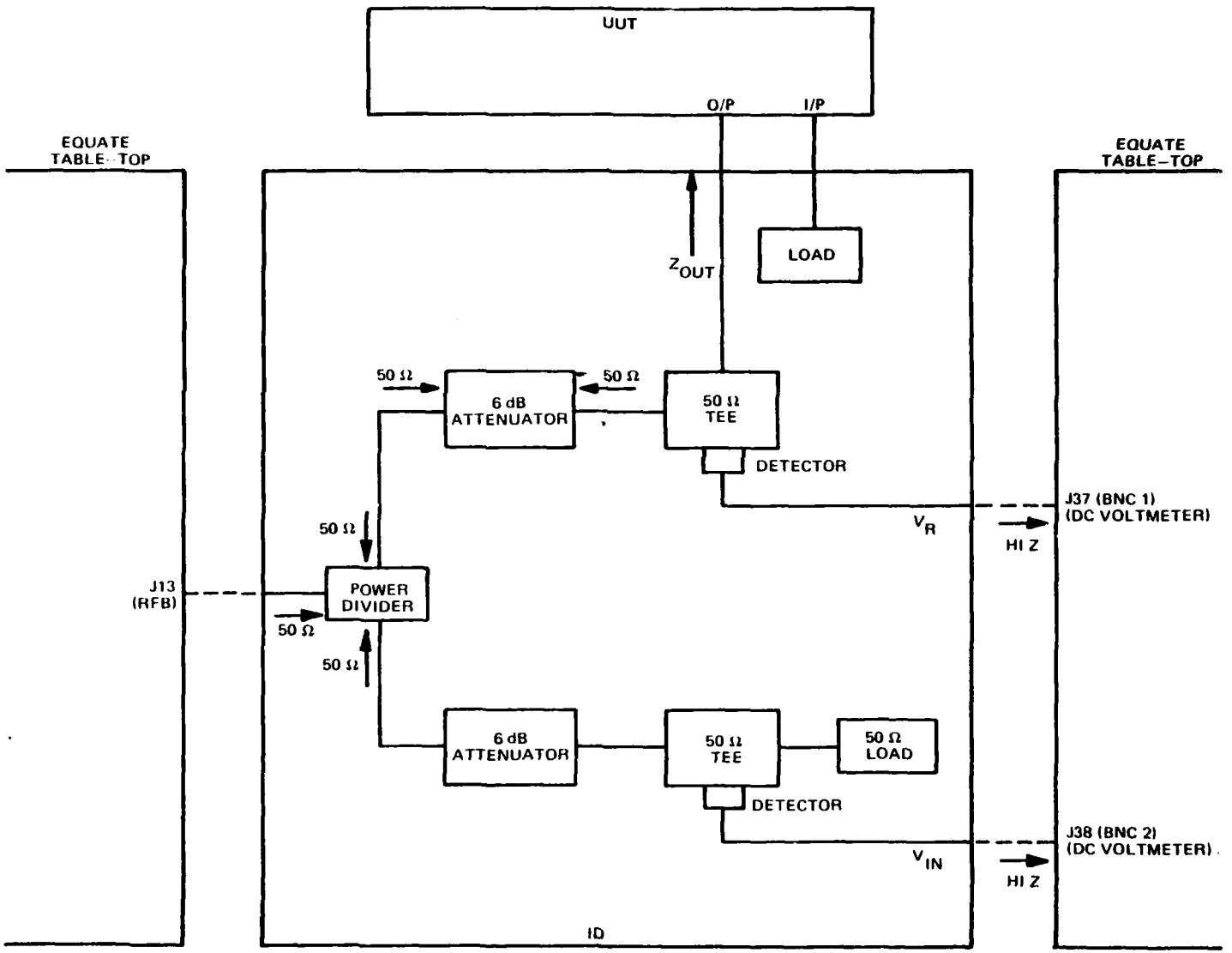


Figure 2-22. ID Diagram: Filter Output Impedance Measurement (60 kHz - 100 MHz)

At the execution of the test program, UUT output is measured in millivolts RMS for each applied frequency. Insertion loss in DB is automatically calculated for each frequency using the following equation:

Insertion loss (DB) = 20 LOG (VIN/MVOUT) - (MATCHIN + MATCHOT)

where VIN = Signal amplitude in millivolts RMS from waveform generator to ID as UUT input

MVOUT = Measured output voltages in millivolts RMS

MATCHIN = Insertion loss in DB of the input matching network

MATCHOT = Insertion loss in DB of the output matching network

The measured insertion loss values in the passband region are compared with the maximum loss specification while the measured values in stopband are compared to minimum rejection specification for the test FAIL/PASS decision.

If 3 DB measurements are desired, the insertion loss at the upper and lower 3 DB frequencies are calculated. The measured insertion loss is compared with the specified value in the passband and must be subtracted by 3 DB for the test PASS/FAIL decision.

2.15.2 Freq. Range 60 KHZ - 100 MHZ

The AGEN user designs the ID according to the ID diagram (fig. 2-24). Matching networks of known insertion loss, as indicated in the ID diagram, may be required in the ID design. The parameters entered to AGEN are the same as in 2.15.1 except the signal amplitude to ID for UUT input is entered in DBM instead of millivolts RMS (RFB is used as the frequency source).

At the execution of the test program, UUT output is measured in millivolts RMS for each applied frequency. The measured output for each applied frequency is automatically converted into DBM using the following equation:

MDBO = 20 LOG (MVOUT/224)

where MDBO = output in DBM

MVOUT = Measured output in millivolts RMS

Insertion loss in DB is then calculated automatically for each frequency using the following equation:

INS LOSS (DB) = DBIN-(MDBO + MATCHOT + MATCHIN)

where DBIN = Signal amplitude in DBM from RFB to ID for UUT input

MDBO = Output in DBM, calculated above

MATCHOT = Insertion loss in DB of the output matching network

MATCHIN = Insertion loss in DB of the input matching network

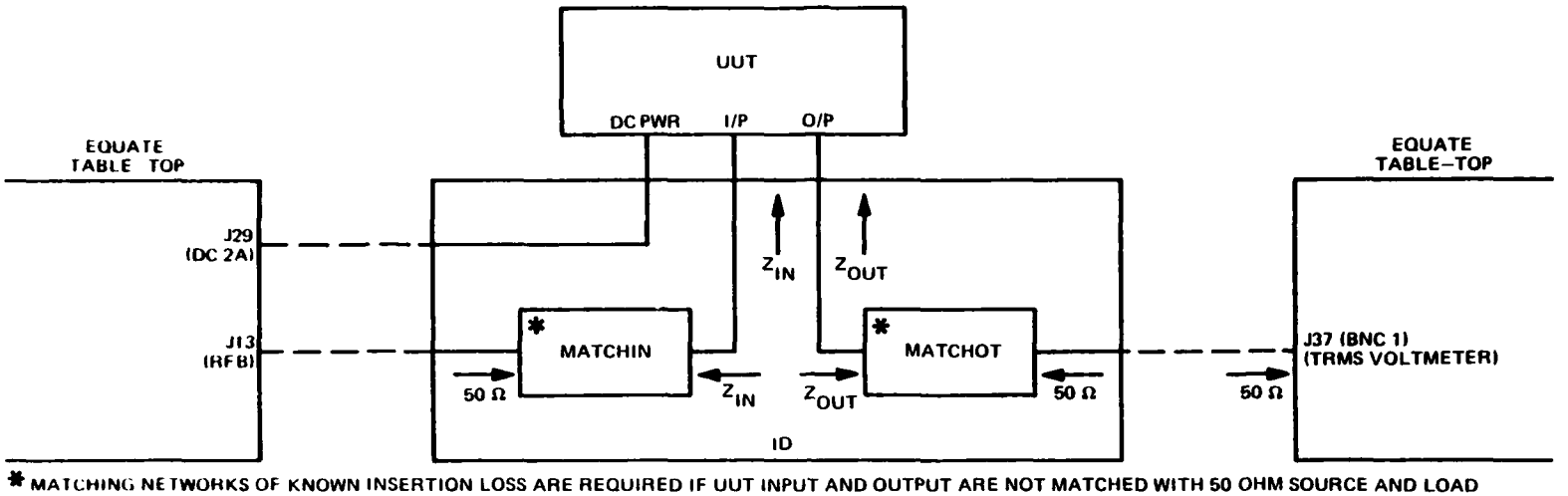


Figure 2-23. ID Diagram: Filter Characteristics Amplitude Response (60 kHz - 100 MHz)

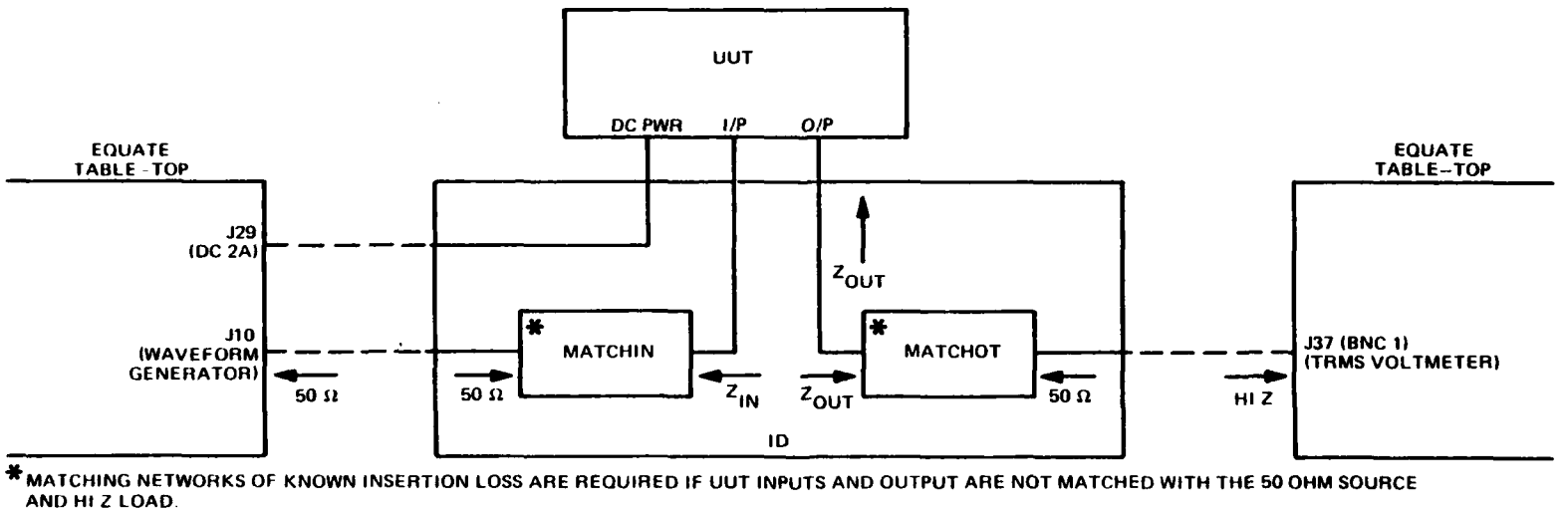


Figure 2-24. ID Diagram: Filter Characteristics Amplitude Response (2 Hz - 1 MHz)

The measured insertion loss values in the passband region are compared with the maximum loss specification while the measured values in stopband are compared to minimum rejection specification for the test FAIL/PASS decision.

If 3 DB measurements are desired, the insertion loss at the upper and lower 3 DB frequencies is automatically calculated. The measured value is compared with the specified value in the passband and must be substracted by 3 DB for the test PASS/FAIL decision.

SECTION III

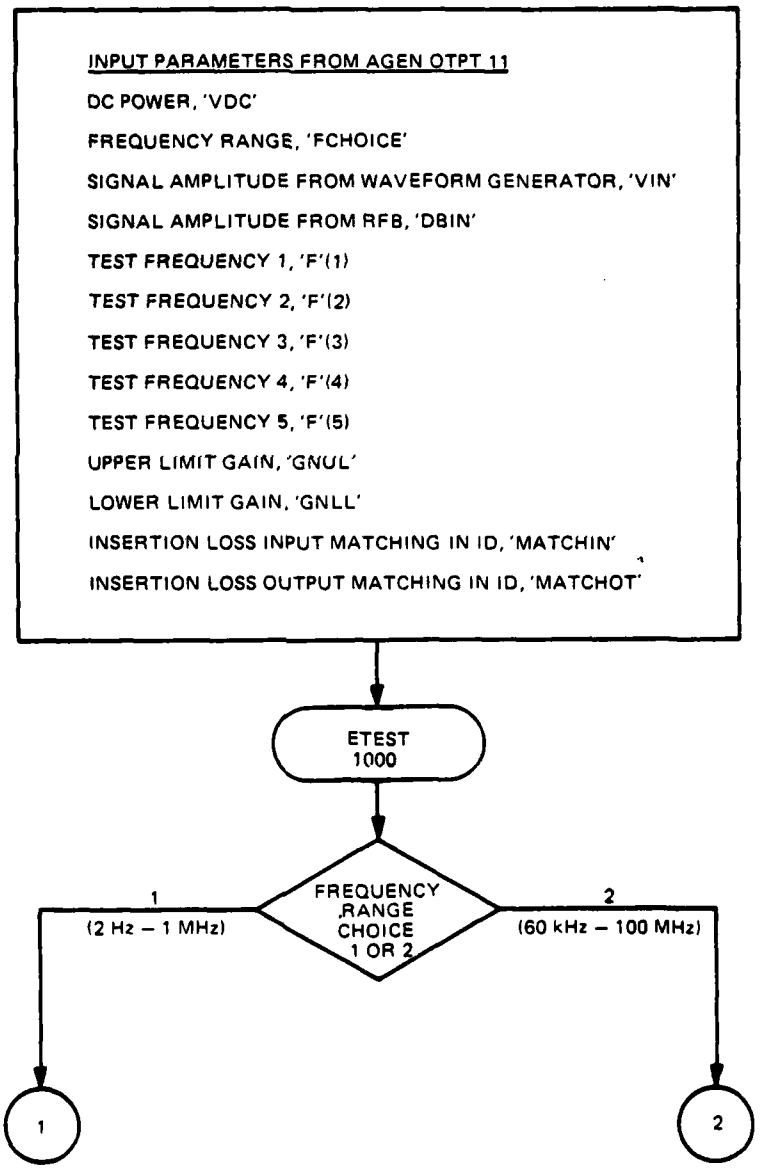
AGEN II Network/Characteristic

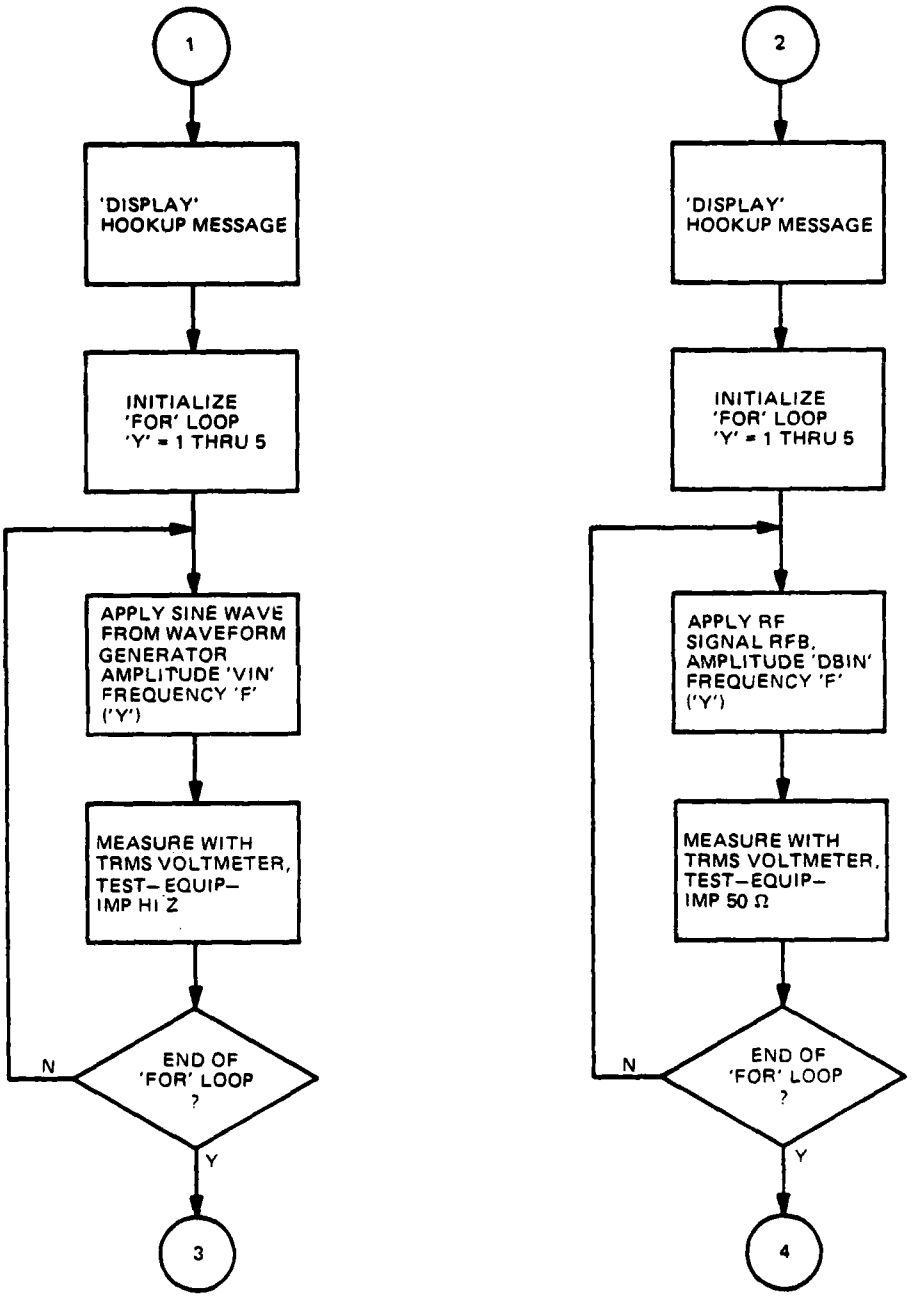
Test Flow Charts

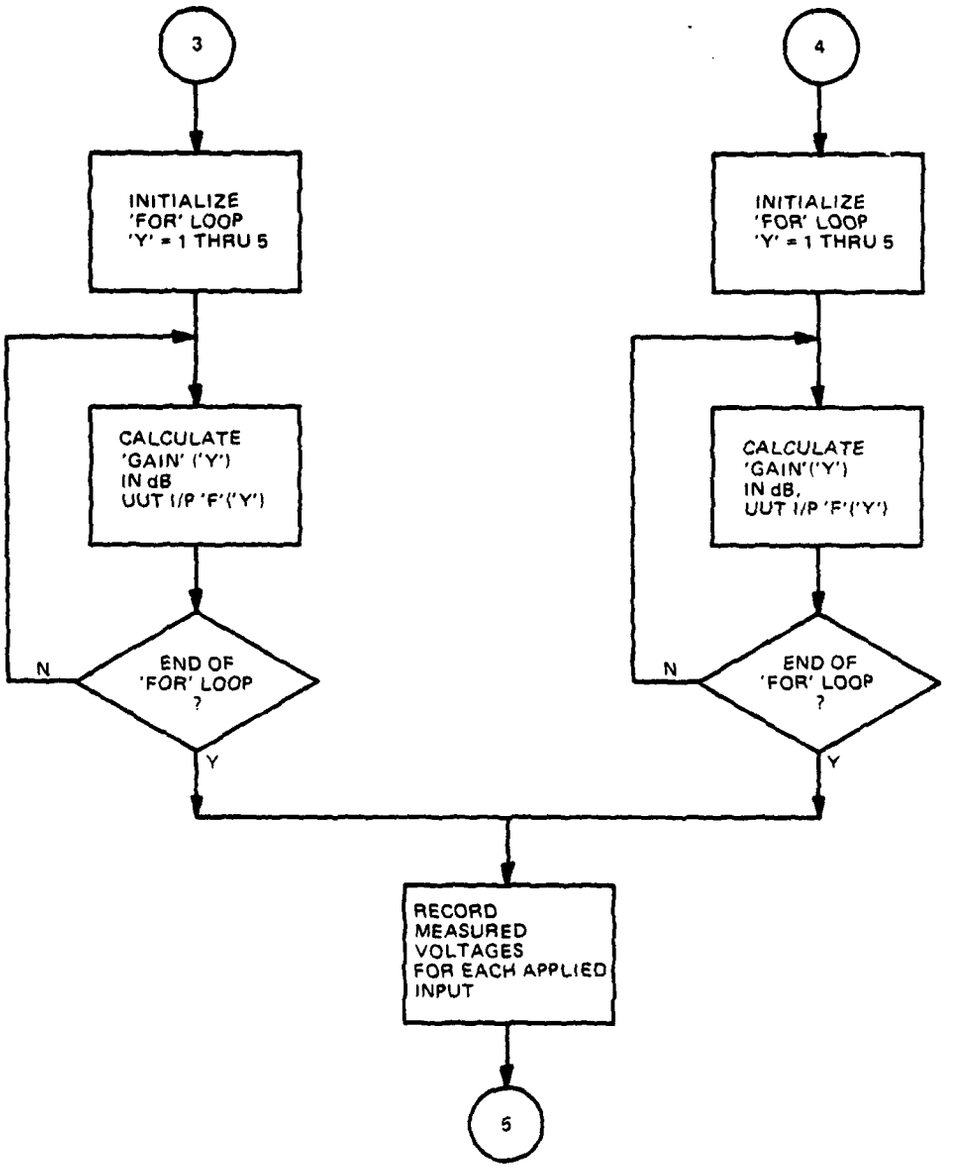
SECTION III

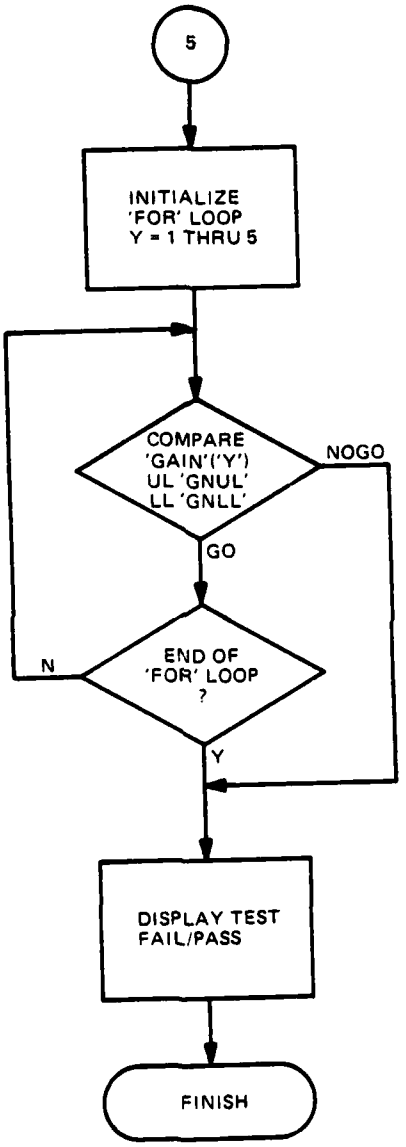
AGEN II NETWORK/CHARACTERISTIC TEST FLOW CHART

3.1 Amplifier Response Test Flow Chart

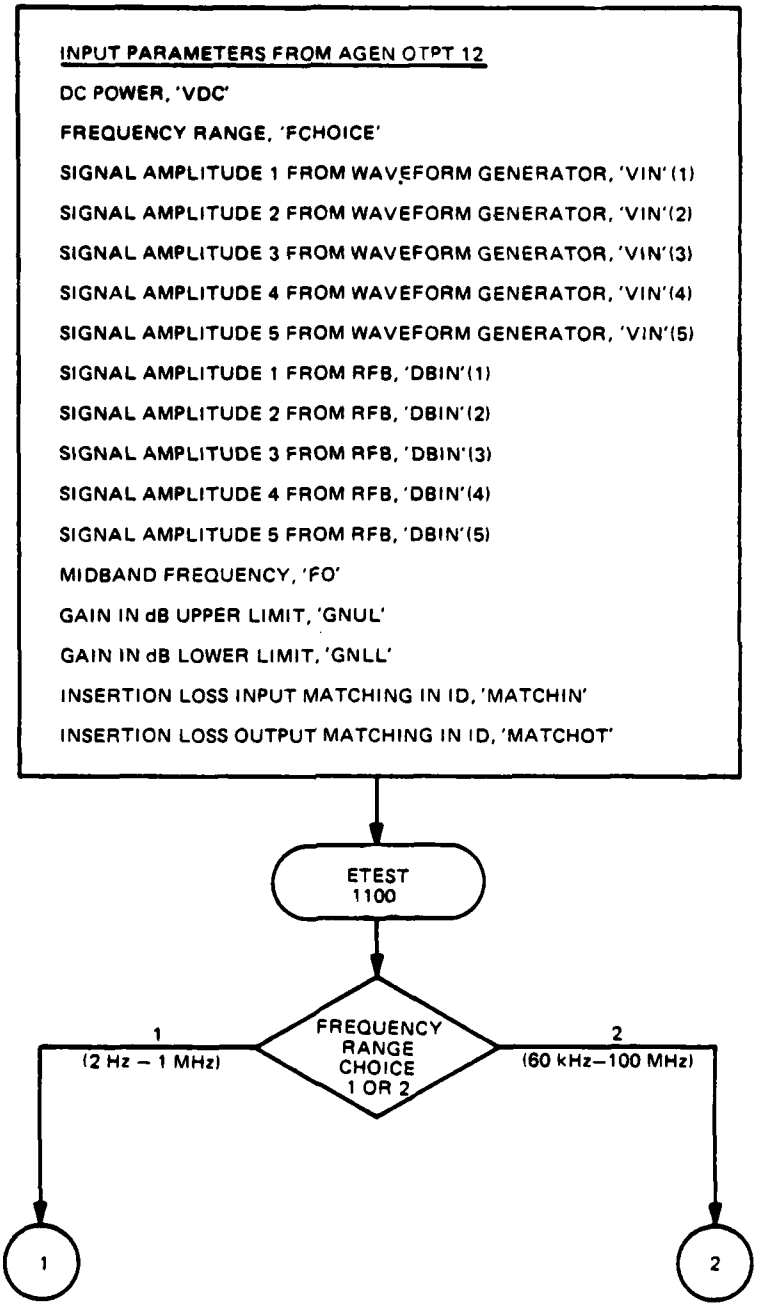


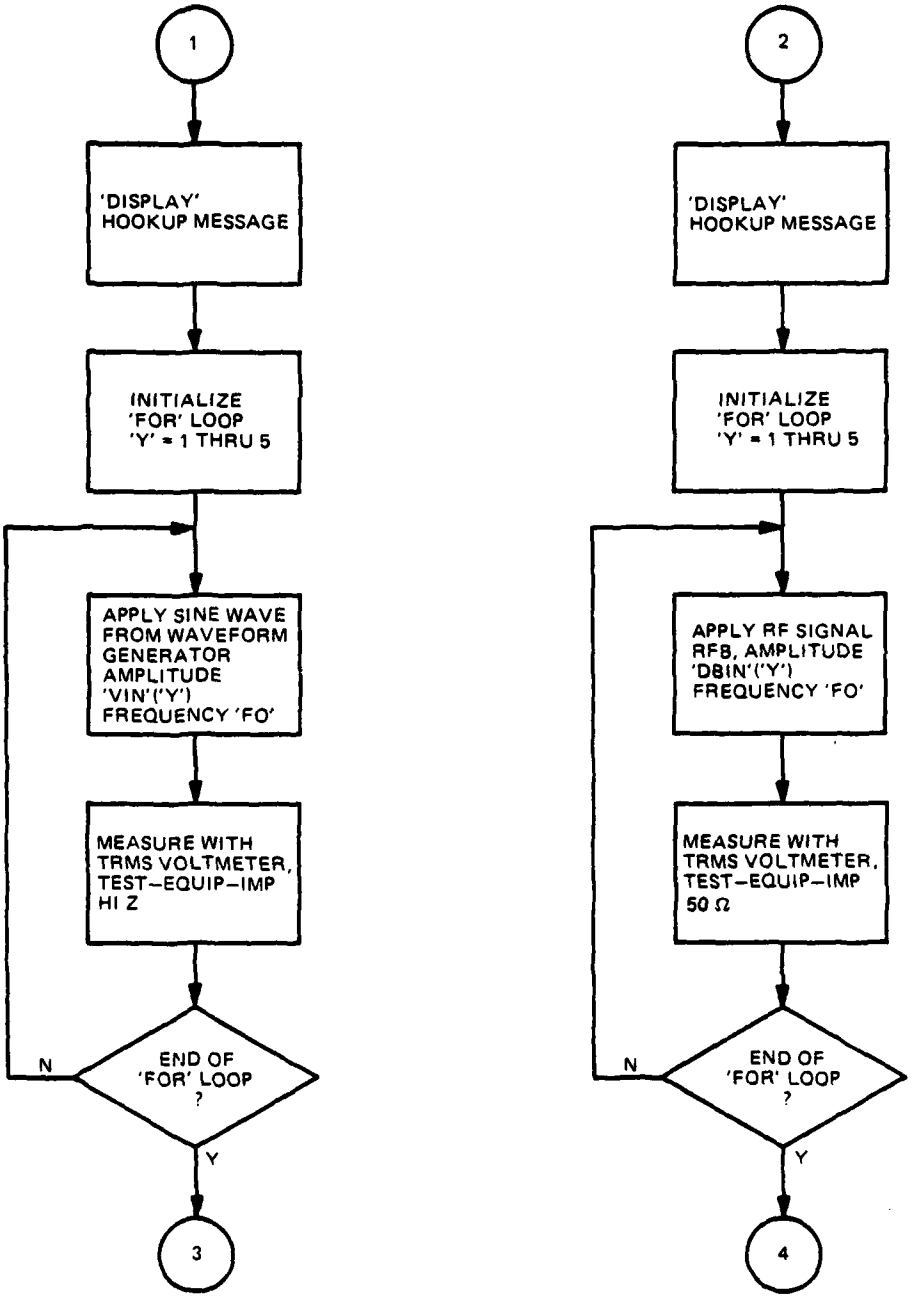

1
'DISPLAY' HOOKUP MESSAGE
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
APPLY SINE WAVE FROM WAVEFORM GENERATOR AMPLITUDE 'VIN' FREQUENCY 'F' ('Y')
MEASURE WITH TRMS VOLTMETER, TEST–EQUIP– IMP HI Z
END OF 'FOR' LOOP ?
N
Y
3
2
'DISPLAY' HOOKUP MESSAGE
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
APPLY RF SIGNAL RFB, AMPLITUDE 'DBIN' FREQUENCY 'F' ('Y')
MEASURE WITH TRMS VOLTMETER, TEST–EQUIP– IMP 50 Ω
END OF 'FOR' LOOP ?
N
Y
4

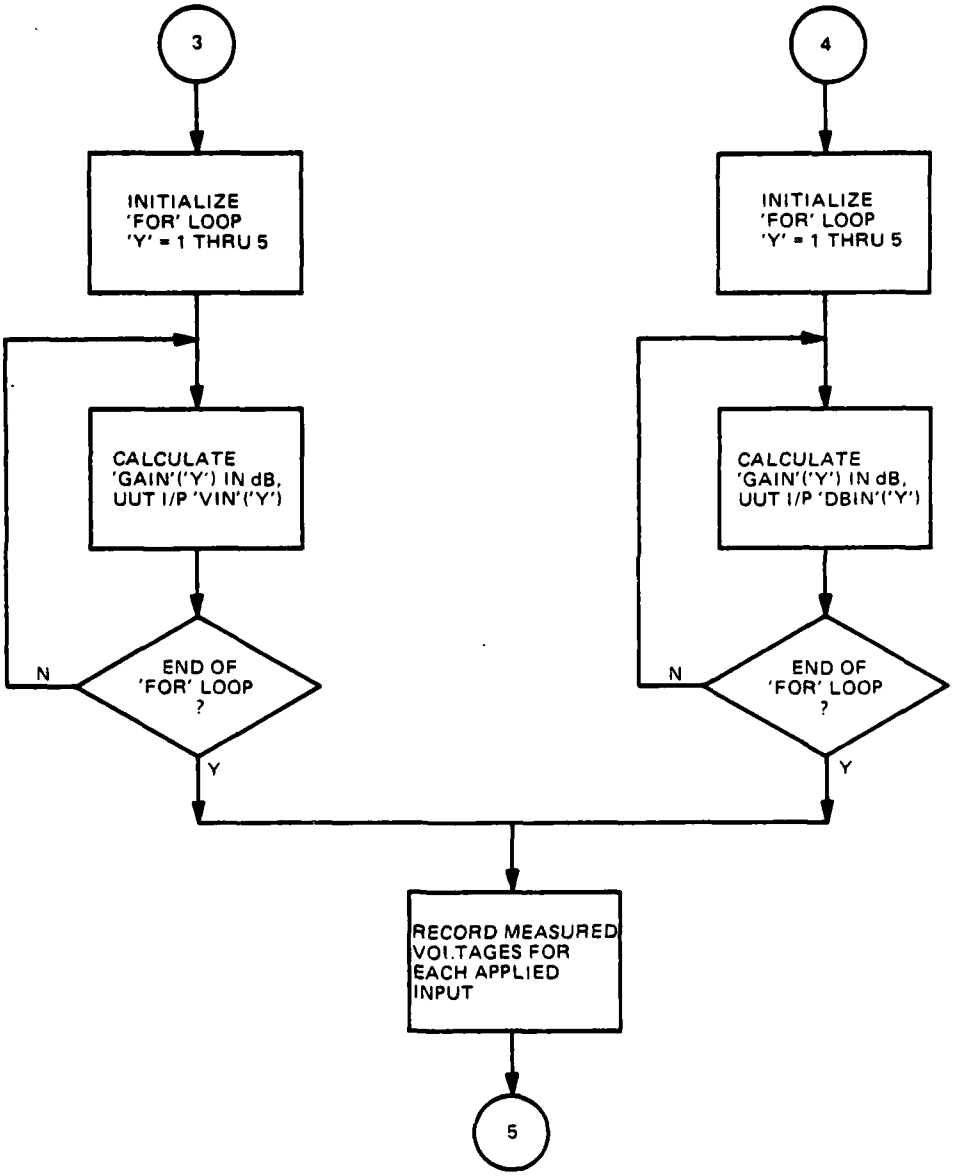

3
4
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
CALCULATE 'GAIN' ('Y') IN dB UUT I/P 'F'('Y')
CALCULATE 'GAIN'('Y') IN dB, UUT I/P 'F'('Y')
N
END OF 'FOR' LOOP ?
N
END OF 'FOR' LOOP ?
Y
Y
RECORD MEASURED VOLTAGES FOR EACH APPLIED INPUT
5

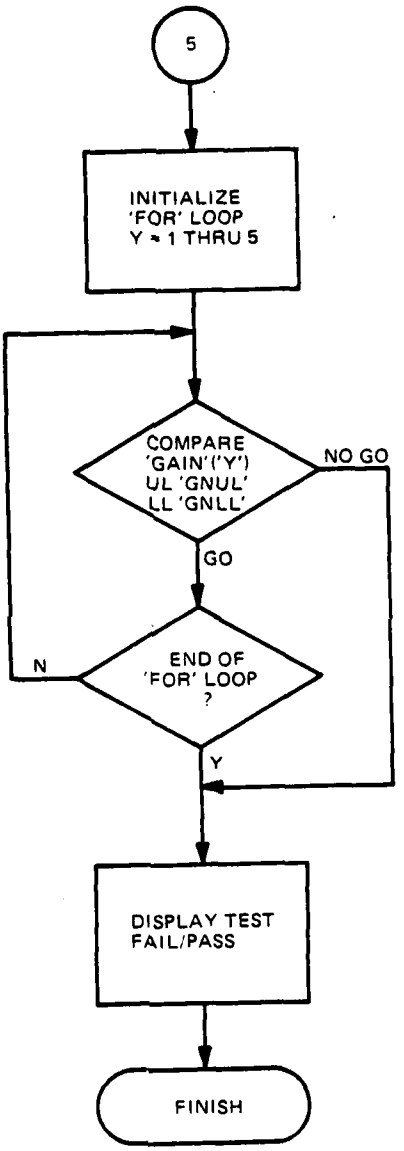

5
INITIALIZE
'FOR' LOOP
Y = 1 THRU 5
COMPARE
'GAIN'('Y')
UL 'GNUL'
LL 'GNLL'
NOGO
GO
END OF
'FOR' LOOP
?
N
Y
DISPLAY TEST
FAIL/PASS
FINISH

3.2 Amplifier Linearity Test Flow Chart

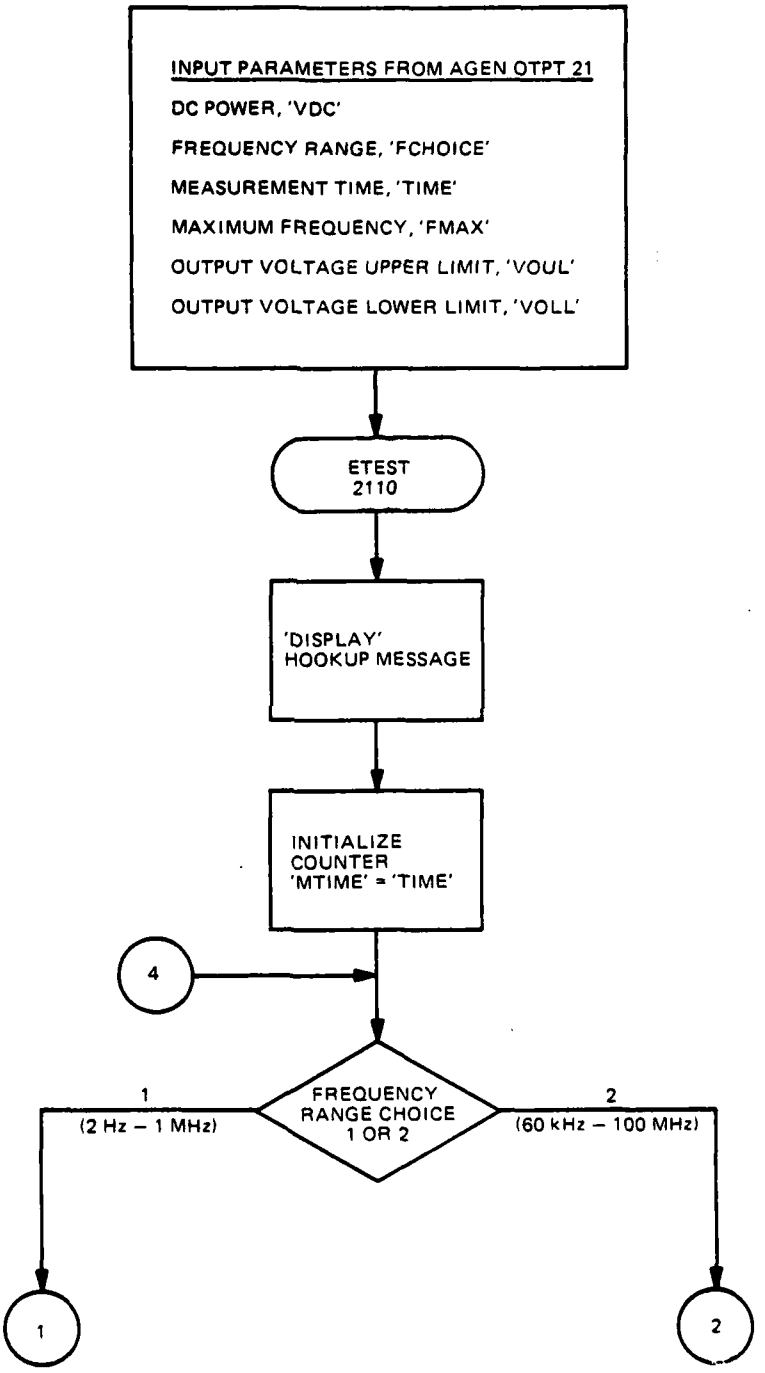


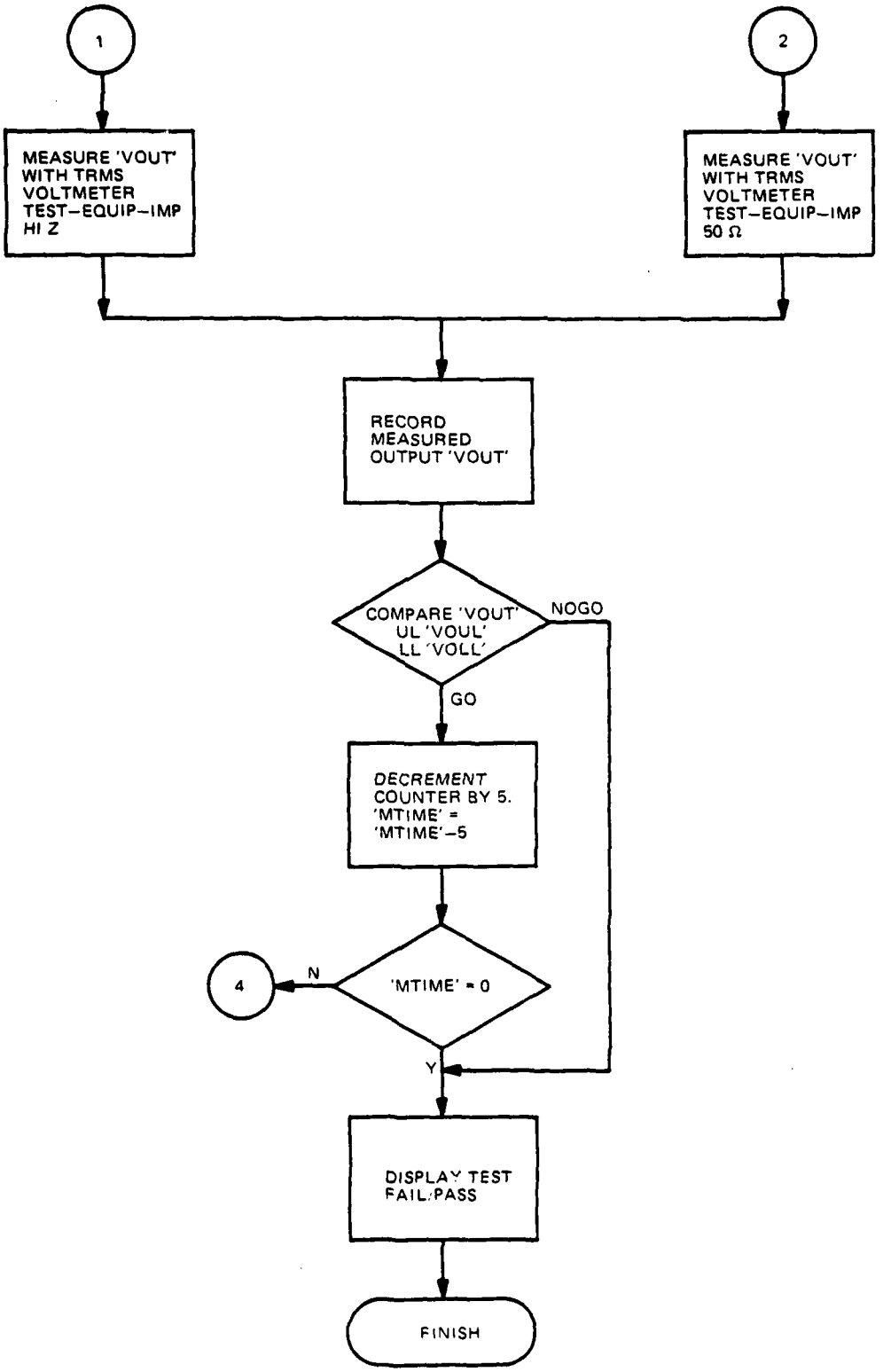

1
'DISPLAY'
HOOKUP MESSAGE
INITIALIZE
'FOR' LOOP
'Y' = 1 THRU 5
APPLY SINE WAVE
FROM WAVEFORM
GENERATOR
AMPLITUDE
'VIN'('Y')
FREQUENCY 'FO'
MEASURE WITH
TRMS VOLTMETER,
TEST-EQUIP-IMP
HI Z
END OF
'FOR' LOOP
?
N
Y
3
2
'DISPLAY'
HOOKUP MESSAGE
INITIALIZE
'FOR' LOOP
'Y' = 1 THRU 5
APPLY RF SIGNAL
RF8, AMPLITUDE
'DBIN'('Y')
FREQUENCY 'FO'
MEASURE WITH
TRMS VOLTMETER,
TEST-EQUIP-IMP
50 Ω
END OF
'FOR' LOOP
?
N
Y
4


3
4
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
CALCULATE 'GAIN'('Y') IN dB, UUT I/P 'VIN'('Y')
CALCULATE 'GAIN'('Y') IN dB, UUT I/P 'DBIN'('Y')
N
END OF 'FOR' LOOP ?
N
END OF 'FOR' LOOP ?
Y
Y
RECORD MEASURED VOLTAGES FOR EACH APPLIED INPUT
5

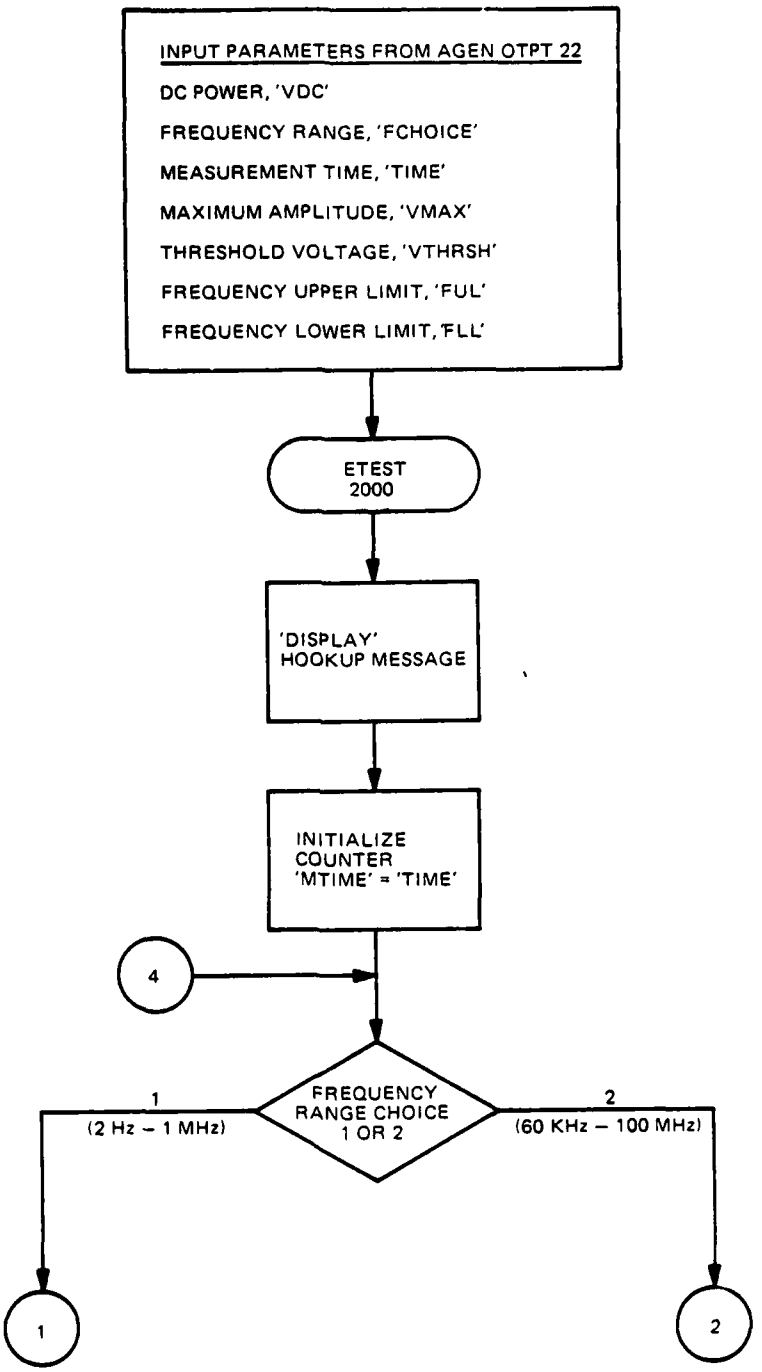

5
INITIALIZE
'FOR' LOOP
Y = 1 THRU 5
COMPARE
'GAIN'('Y')
UL 'GNUL'
LL 'GNLL'
NO GO
GO
END OF
'FOR' LOOP
?
N
Y
DISPLAY TEST
FAIL/PASS
FINISH

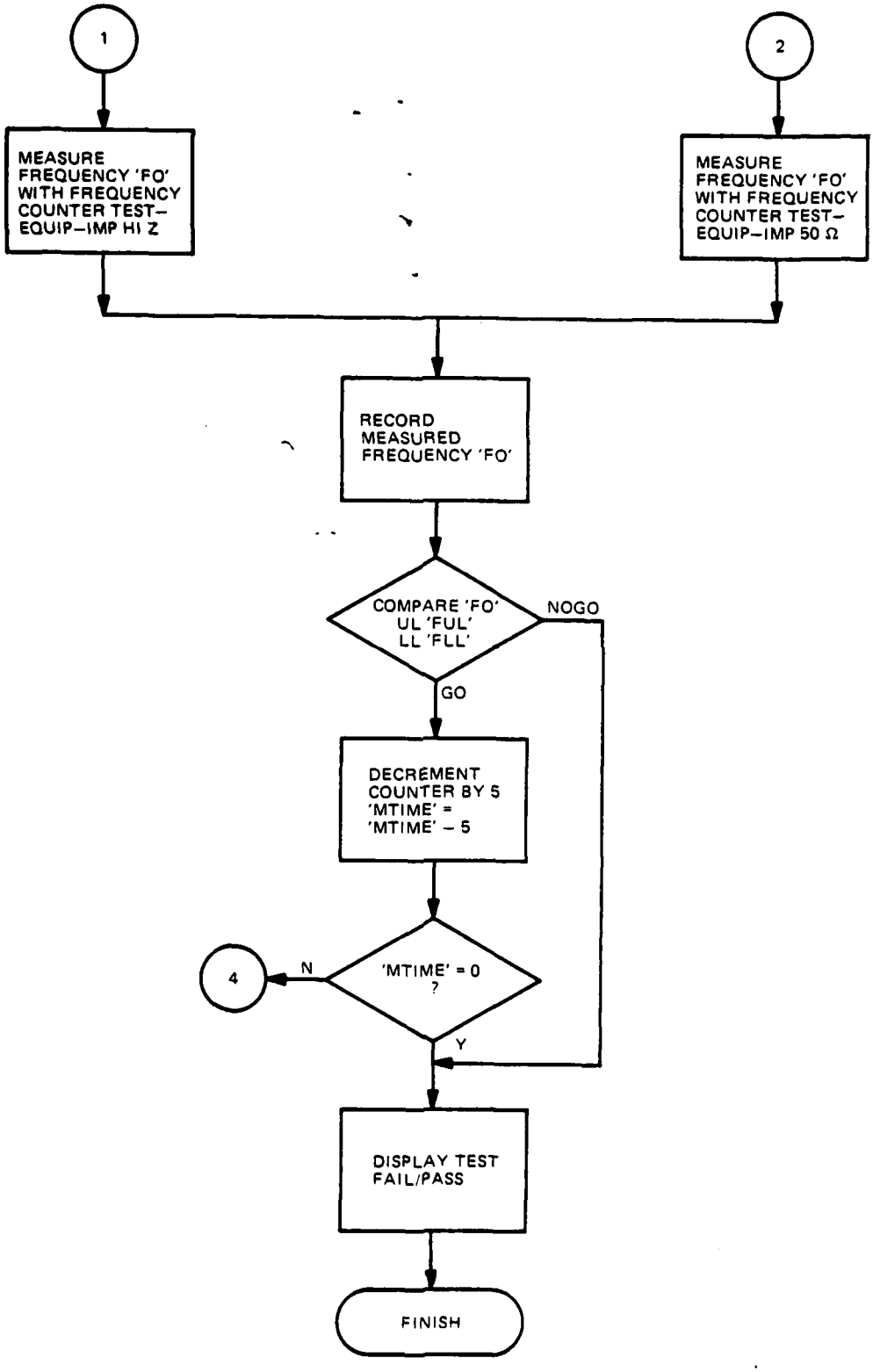
3.3 Oscillator Amplitude Stability Test Flow Chart



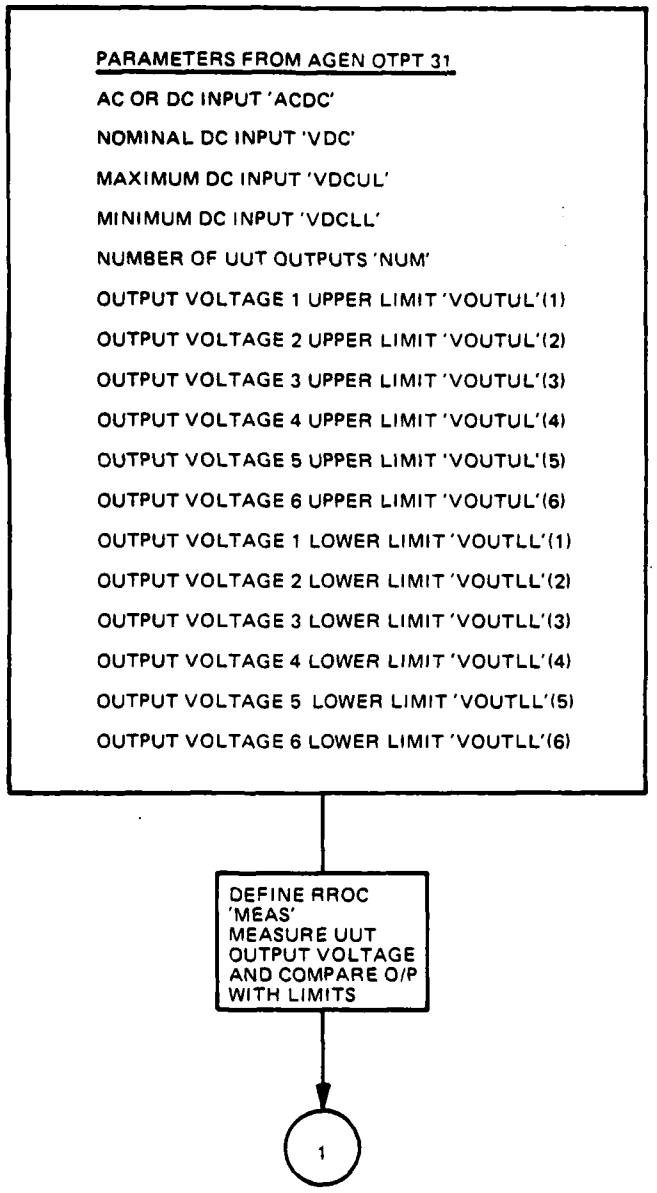

1
2
MEASURE 'VOUT' WITH TRMS VOLTMETER TEST–EQUIP–IMP HI Z
MEASURE 'VOUT' WITH TRMS VOLTMETER TEST–EQUIP–IMP 50 Ω
RECORD MEASURED OUTPUT 'VOUT'
COMPARE 'VOUT' UL 'VOUL' LL 'VOLL'
NOGO
GO
DECREMENT COUNTER BY 5. 'MTIME' = 'MTIME'–5
4
N
'MTIME' = 0
Y
DISPLAY TEST FAIL;PASS
FINISH

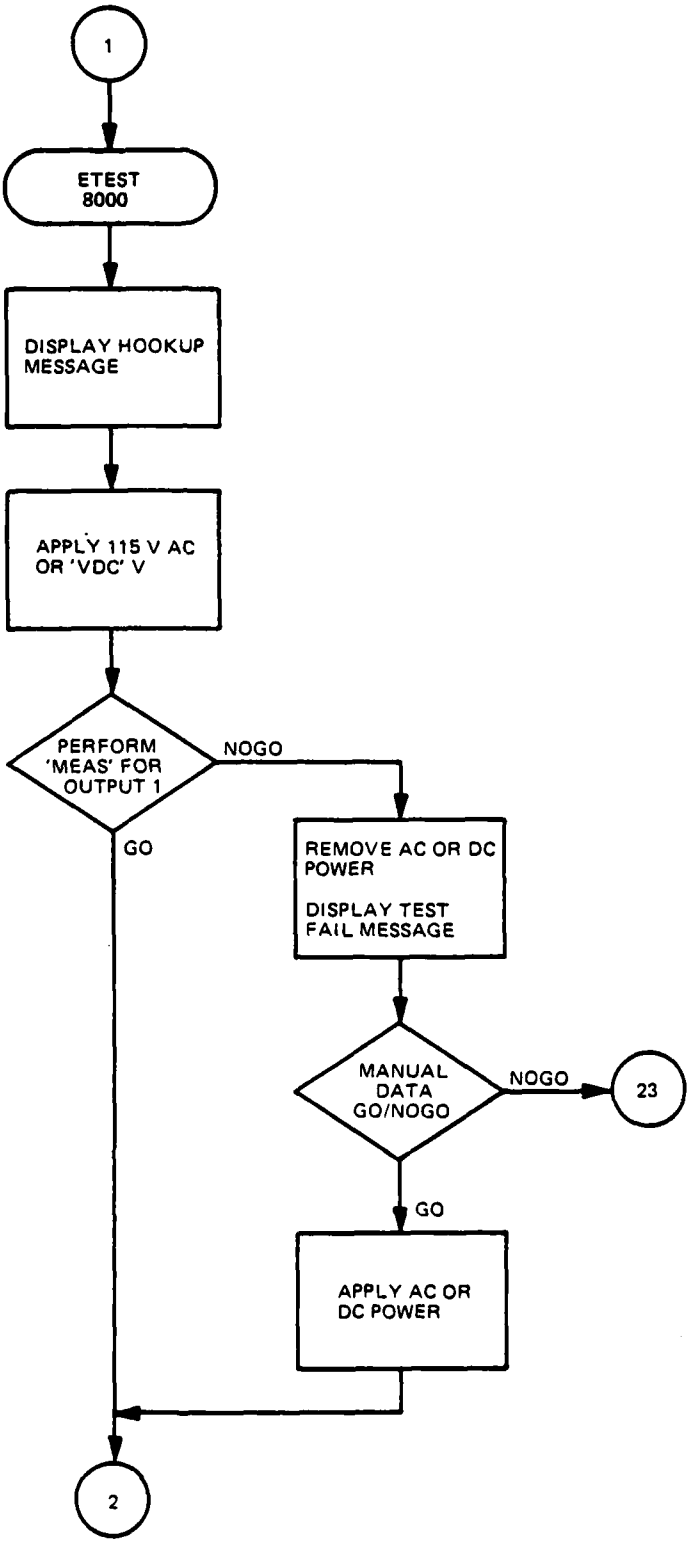
3.4 Oscillator Frequency Stability Test Flow Chart

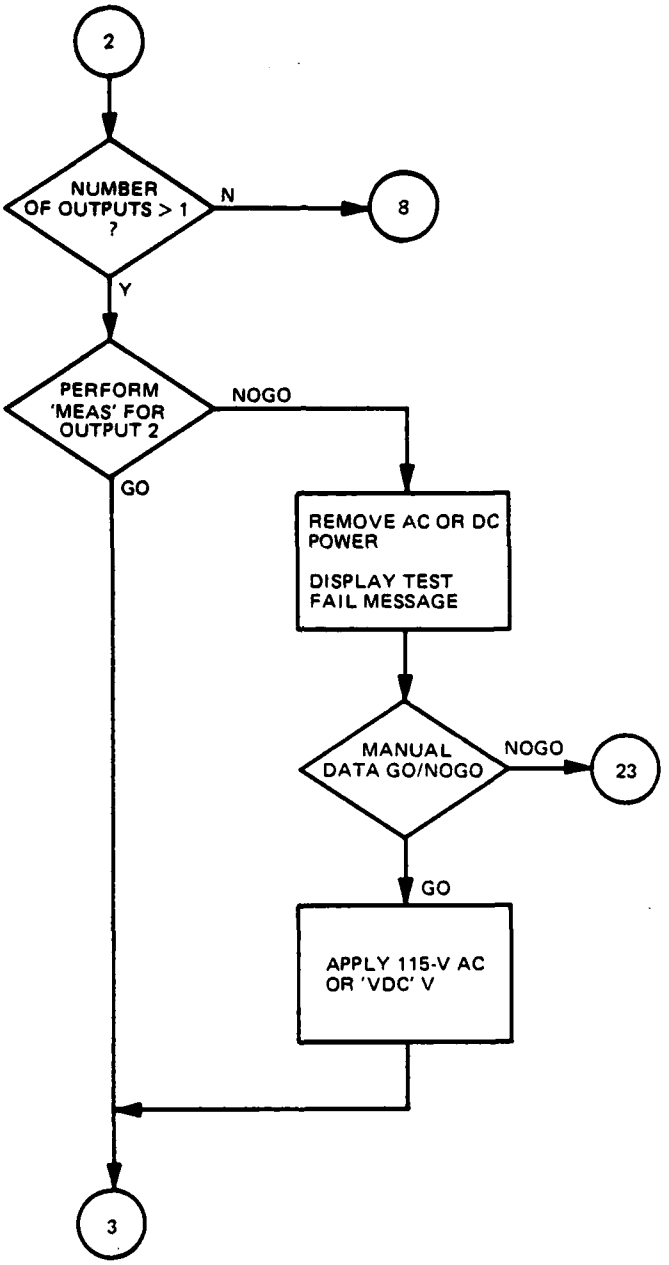


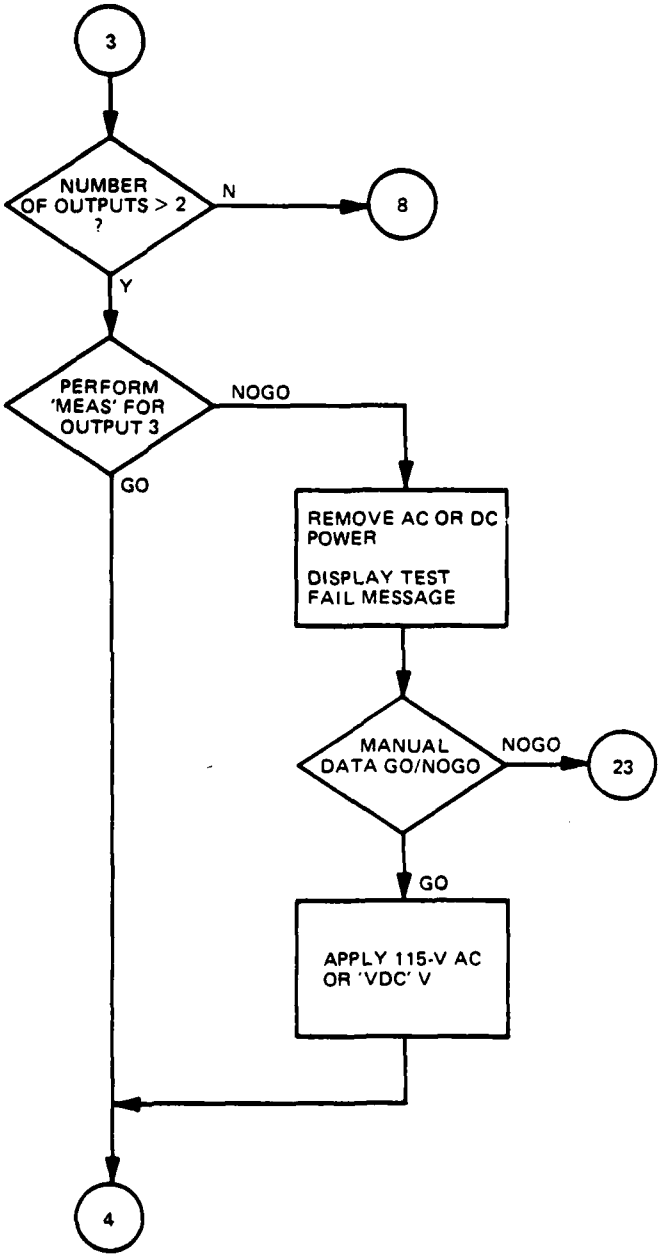

1
2
MEASURE FREQUENCY 'FO' WITH FREQUENCY COUNTER TEST– EQUIP–IMP HI Z
MEASURE FREQUENCY 'FO' WITH FREQUENCY COUNTER TEST– EQUIP–IMP 50 Ω
RECORD MEASURED FREQUENCY 'FO'
COMPARE 'FO' UL 'FUL' LL 'FLL'
NOGO
GO
DECREMENT COUNTER BY 5 'MTIME' = 'MTIME' – 5
4
N
'MTIME' = 0 ?
Y
DISPLAY TEST FAIL/PASS
FINISH

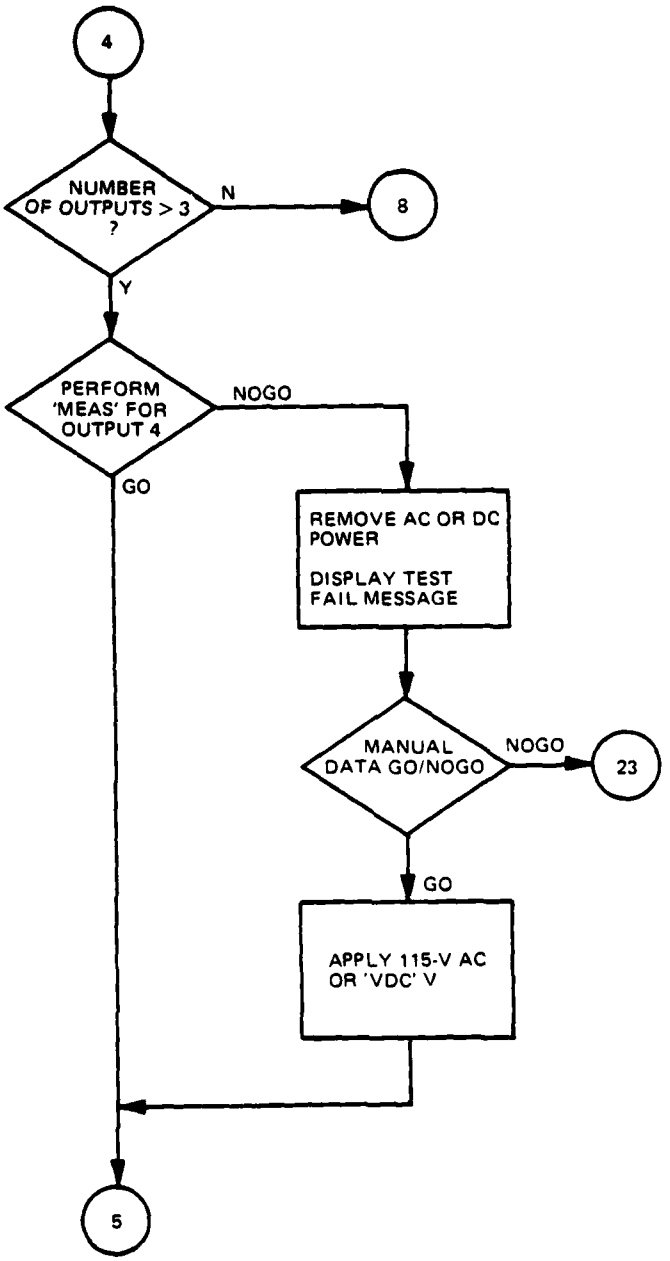
3.5 Power Supply Regulation Test Flow Chart

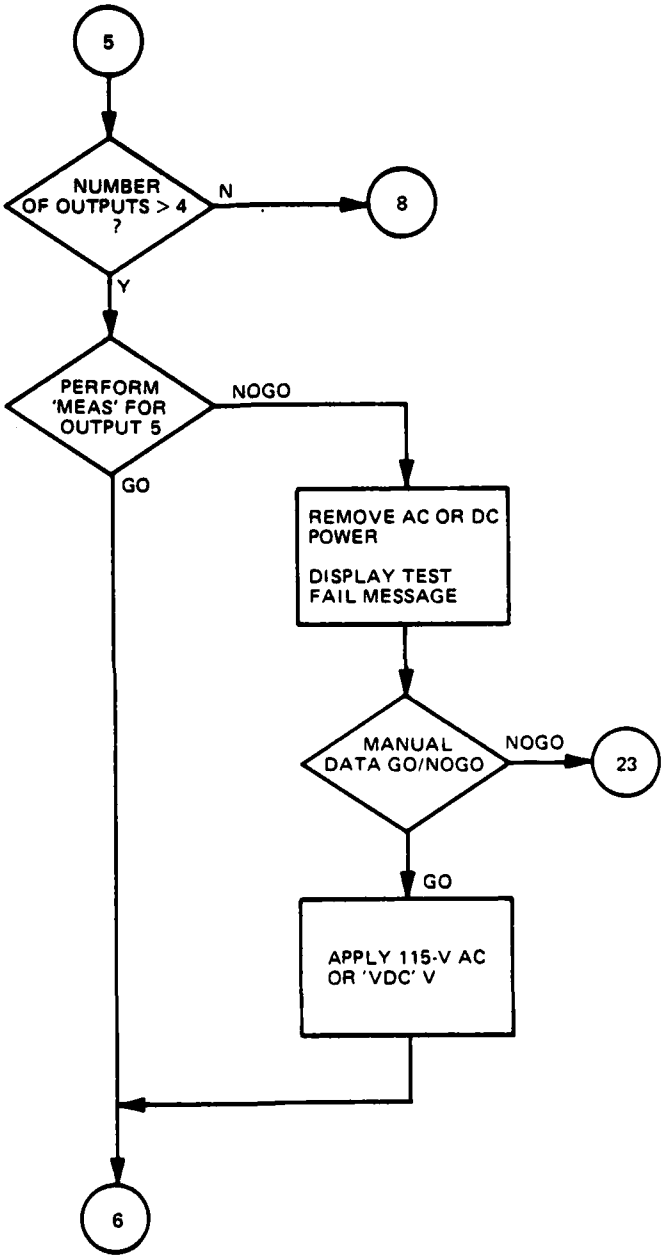


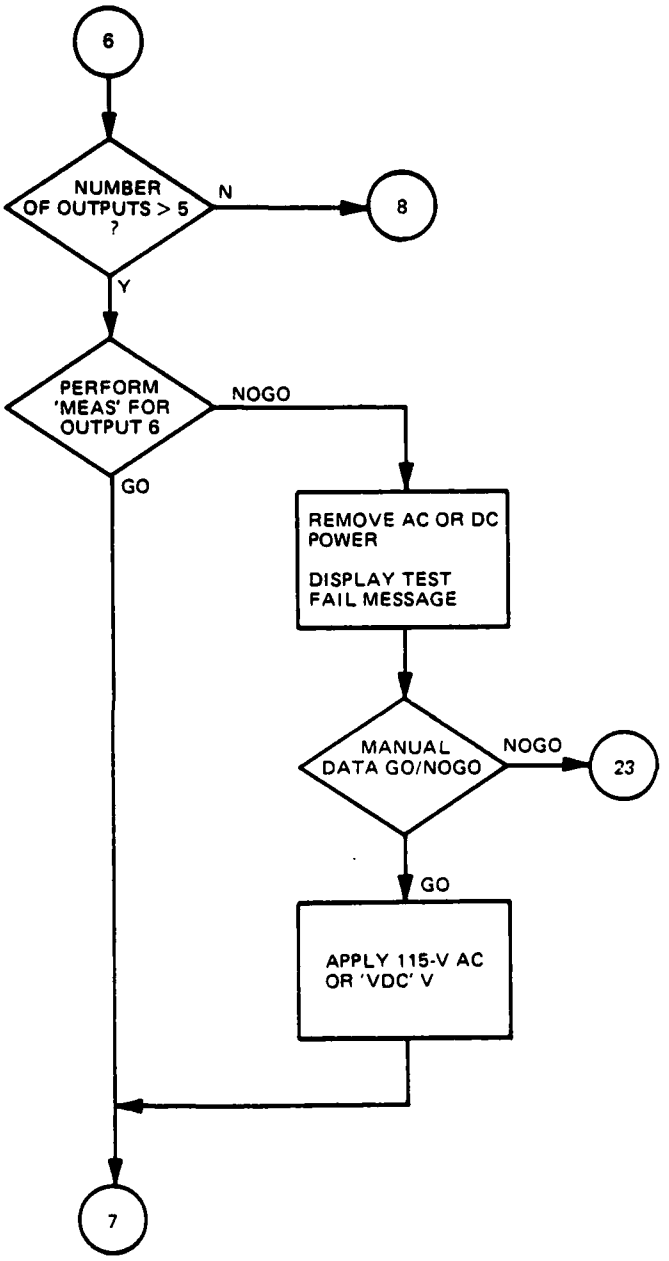

1
ETEST
8000
DISPLAY HOOKUP
MESSAGE
APPLY 115 V AC
OR 'VDC' V
PERFORM
'MEAS' FOR
OUTPUT 1
NOGO
GO
REMOVE AC OR DC
POWER
DISPLAY TEST
FAIL MESSAGE
MANUAL
DATA
GO/NOGO
NOGO
23
GO
APPLY AC OR
DC POWER
2

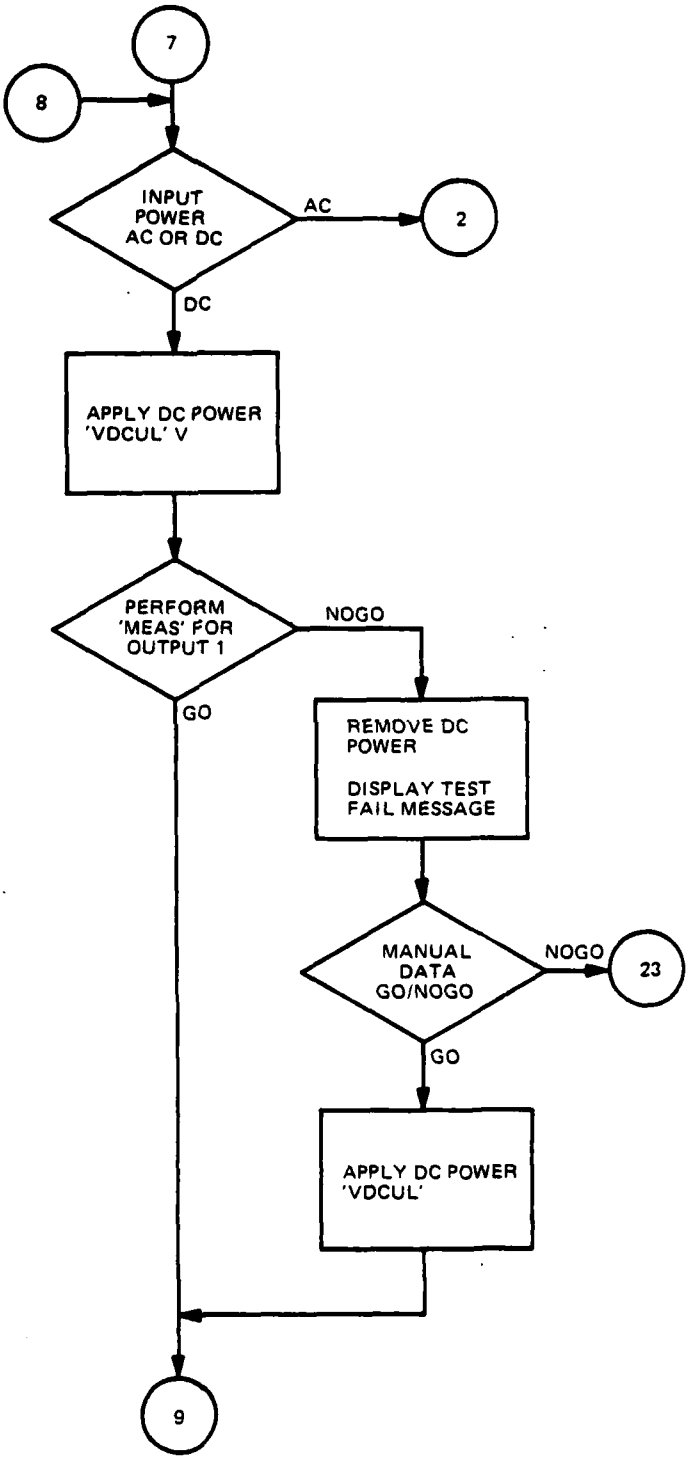

2
NUMBER OF OUTPUTS > 1 ?
N
8
Y
PERFORM 'MEAS' FOR OUTPUT 2
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY 115-V AC OR 'VDC' V
3

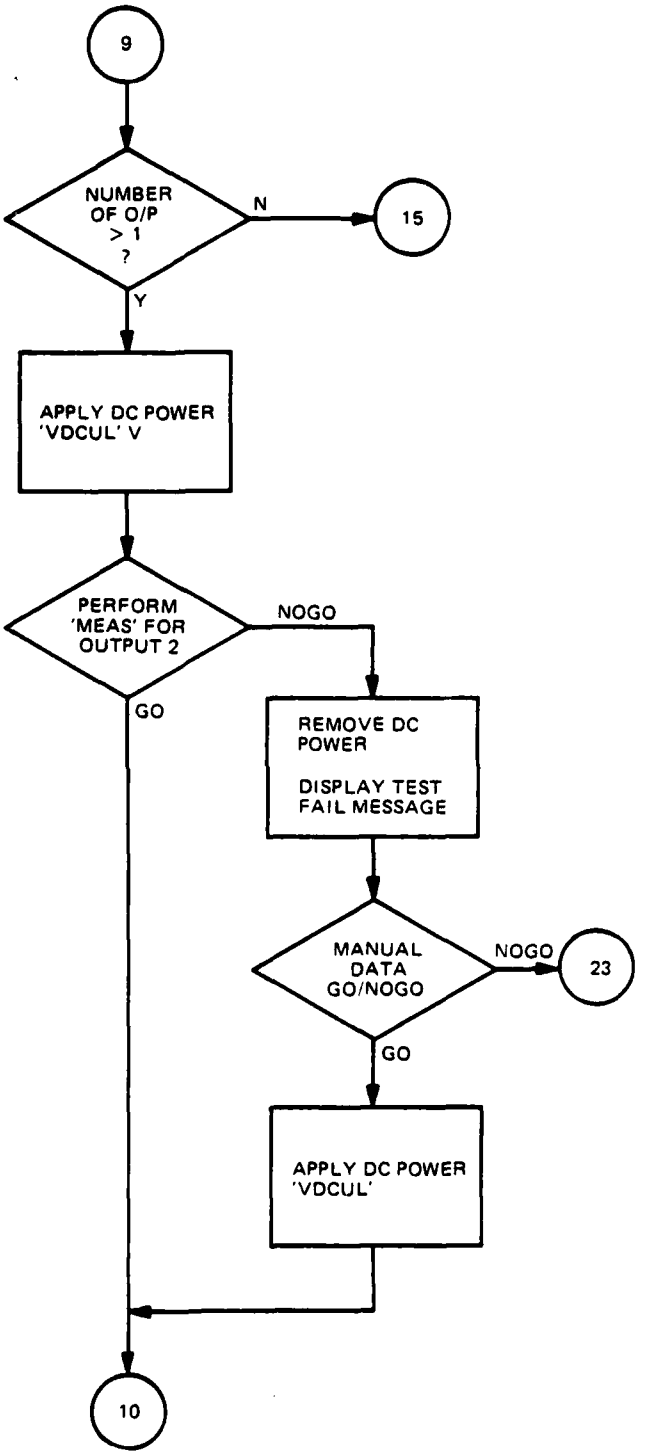

3
NUMBER OF OUTPUTS > 2 ?
N
8
Y
PERFORM 'MEAS' FOR OUTPUT 3
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY 115-V AC OR 'VDC' V
4

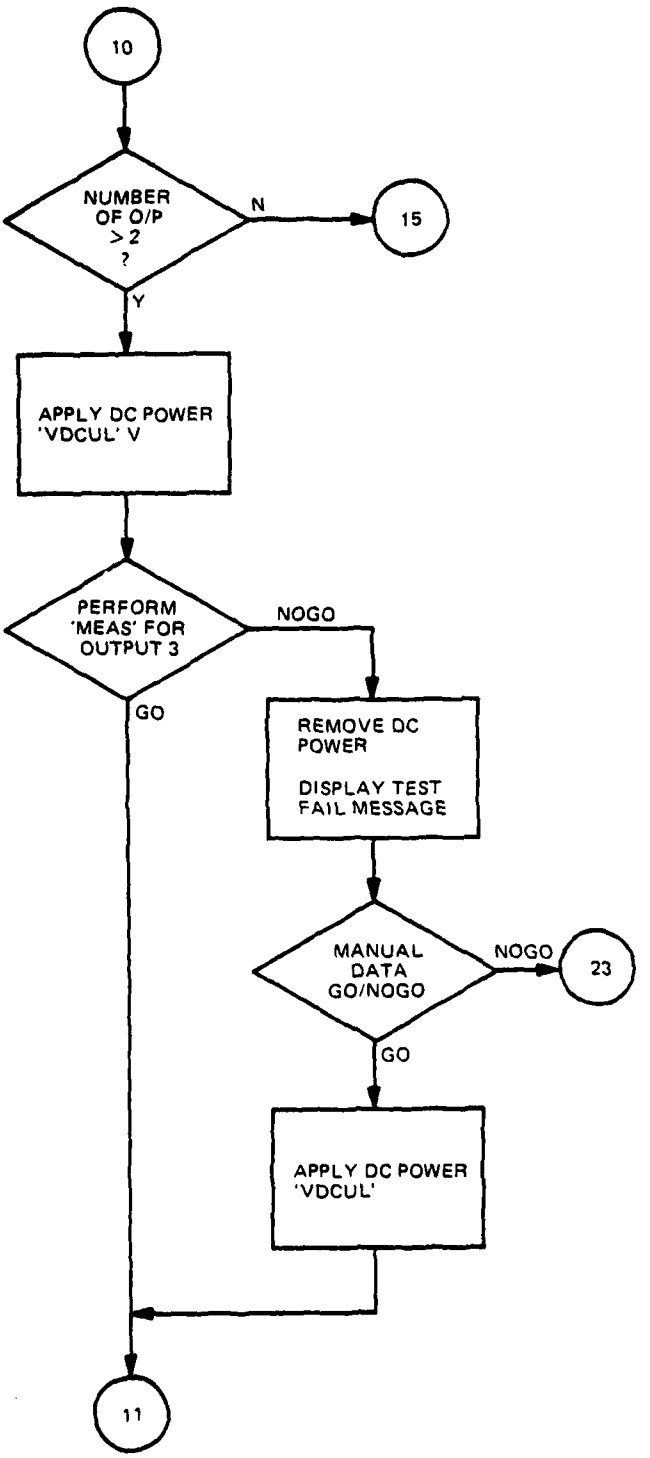

4
NUMBER OF OUTPUTS > 3 ?
N
8
Y
PERFORM 'MEAS' FOR OUTPUT 4
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY 115-V AC OR 'VDC' V
5

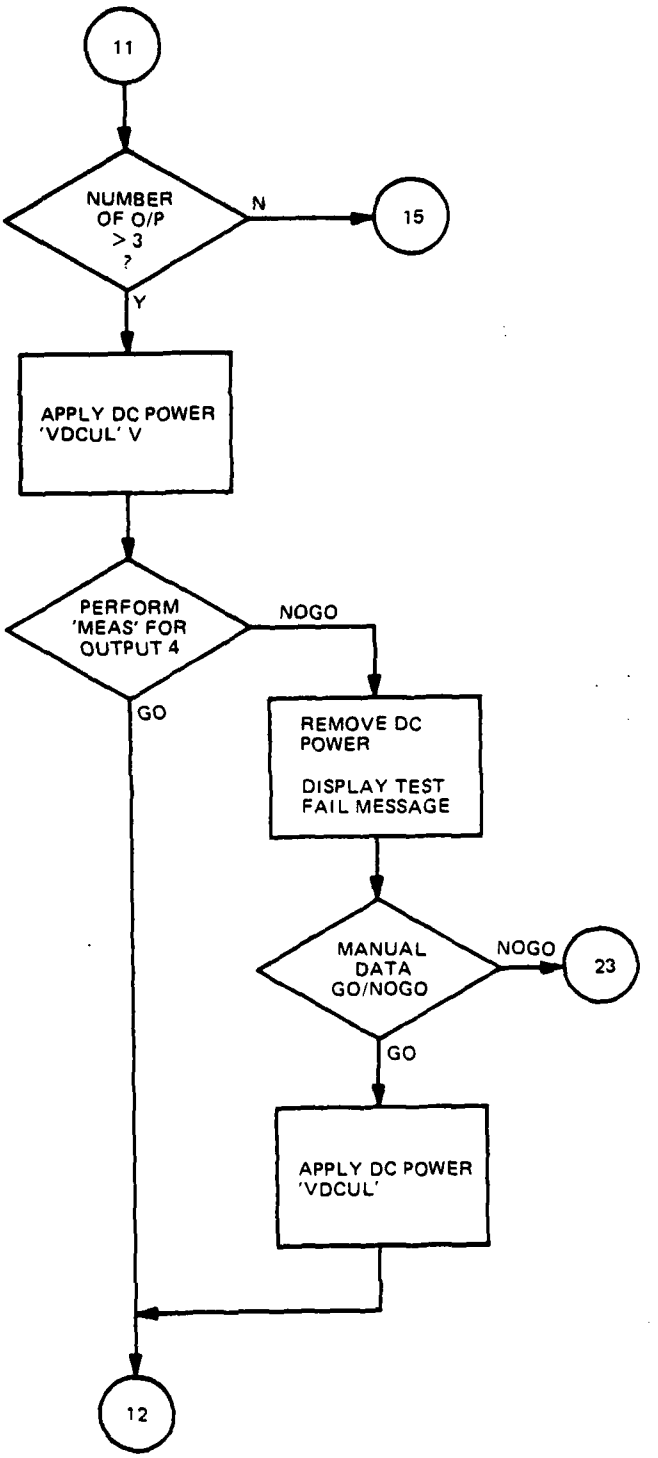

5
NUMBER OF OUTPUTS > 4 ?
N
8
Y
PERFORM 'MEAS' FOR OUTPUT 5
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY 115-V AC OR 'VDC' V
6

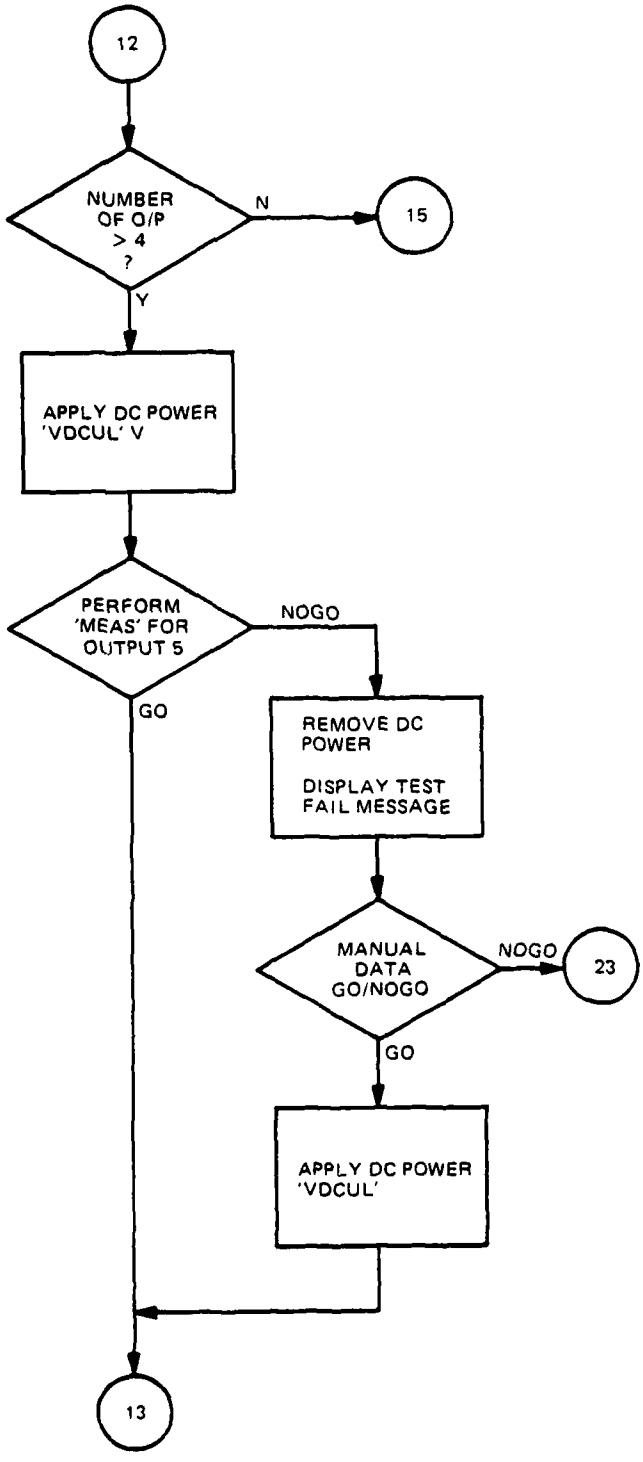

6
NUMBER OF OUTPUTS > 5 ?
N
8
Y
PERFORM 'MEAS' FOR OUTPUT 6
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY 115-V AC OR 'VDC' V
7

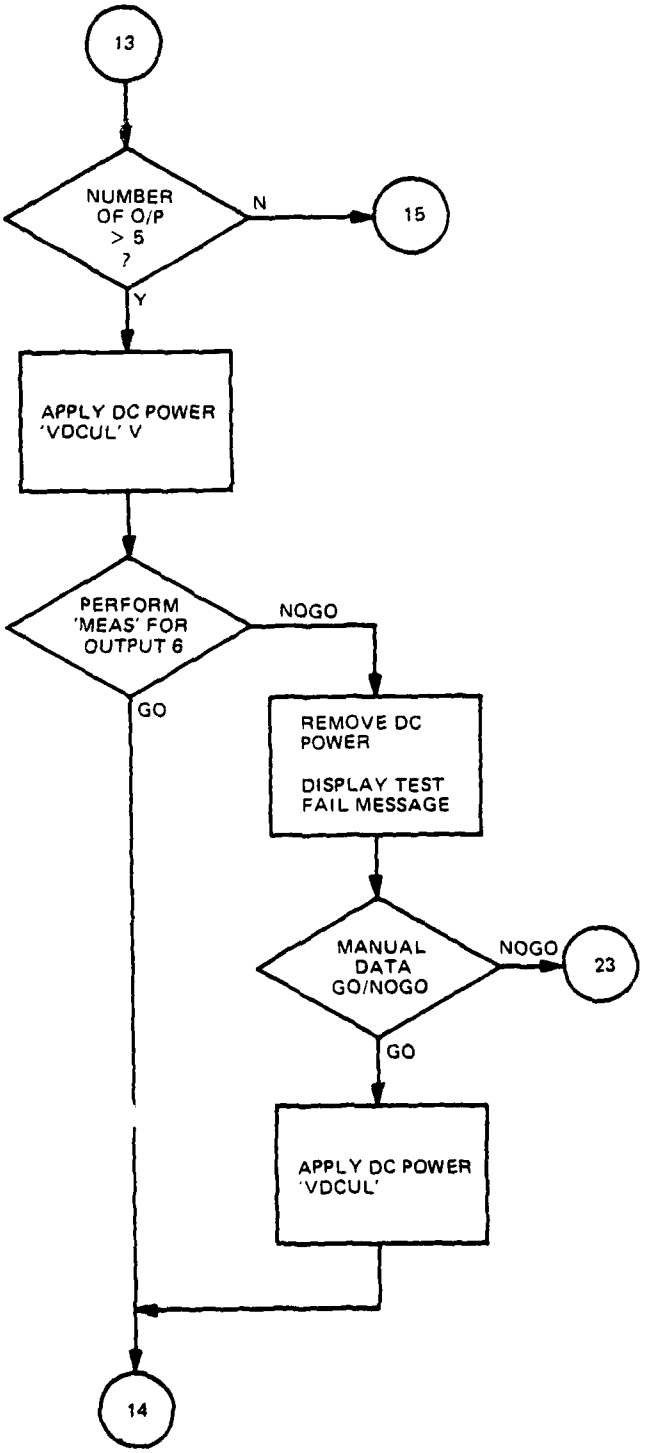

7
8
INPUT POWER AC OR DC
AC
2
DC
APPLY DC POWER 'VDCUL' V
PERFORM 'MEAS' FOR OUTPUT 1
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCUL'
9

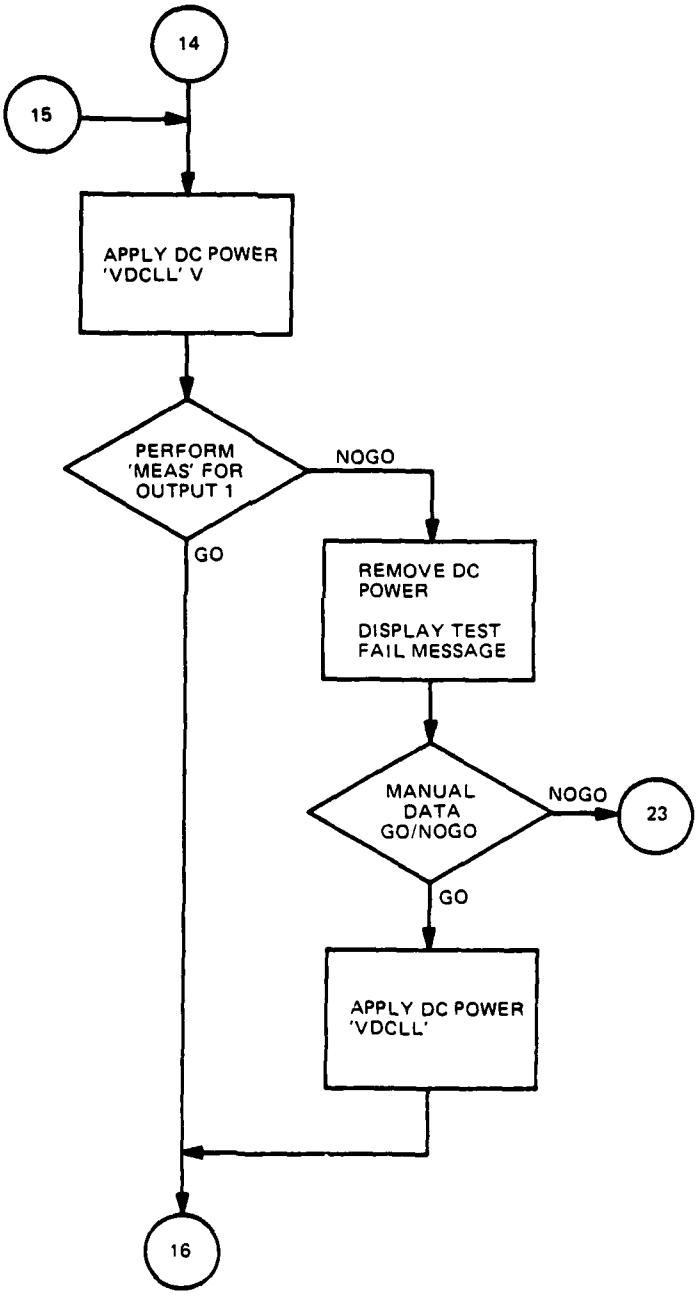

9
NUMBER OF O/P > 1 ?
N
15
Y
APPLY DC POWER 'VDCUL' V
PERFORM 'MEAS' FOR OUTPUT 2
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCUL'
10

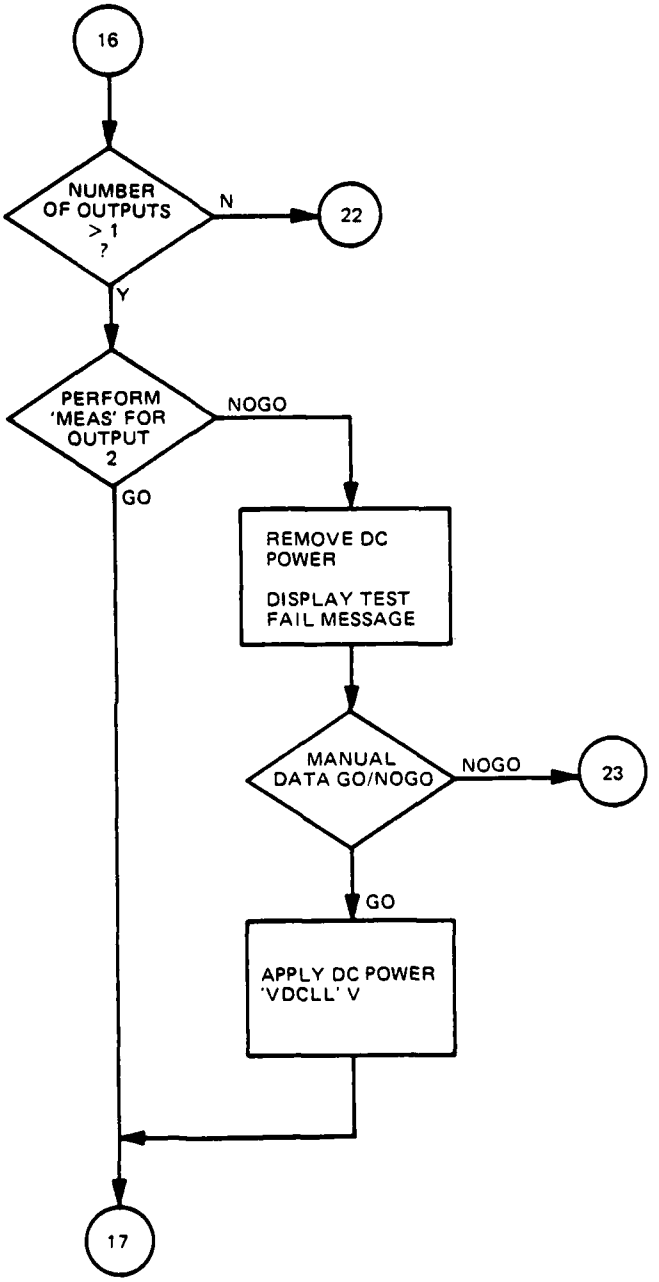

10
NUMBER OF O/P > 2 ?
N
15
Y
APPLY DC POWER 'VDCUL' V
PERFORM 'MEAS' FOR OUTPUT 3
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCUL'
11

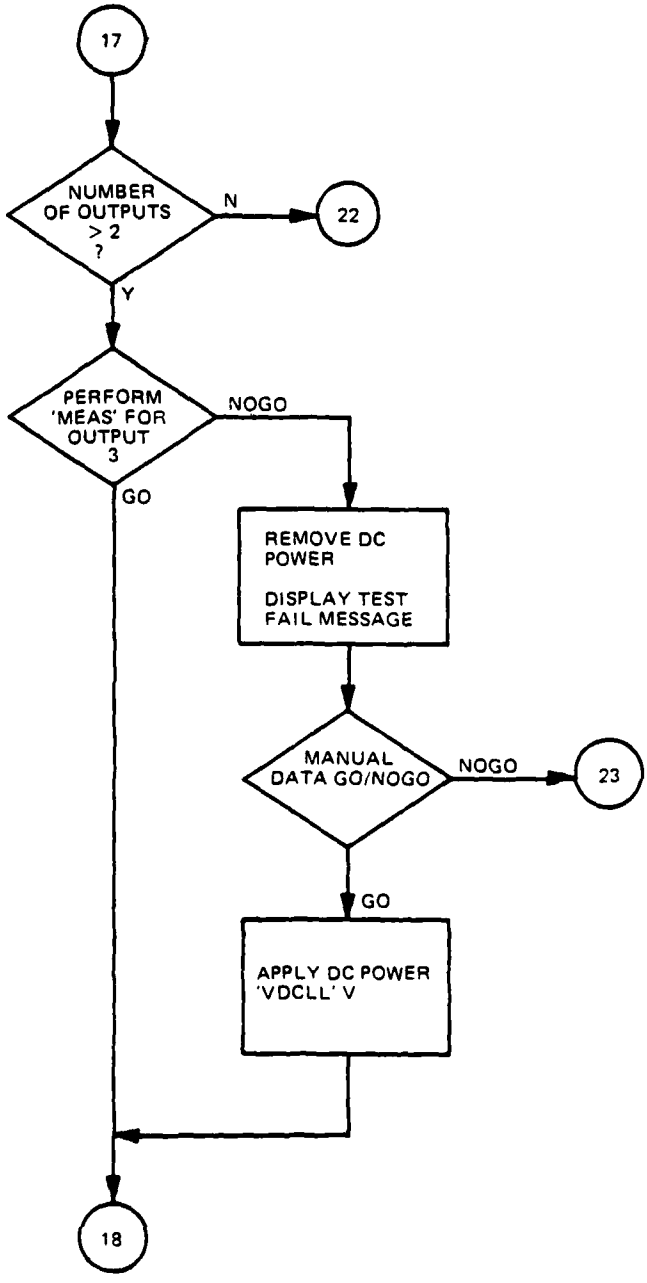

11
NUMBER OF O/P > 3 ?
N
15
Y
APPLY DC POWER 'VDCUL' V
PERFORM 'MEAS' FOR OUTPUT 4
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCUL'
12

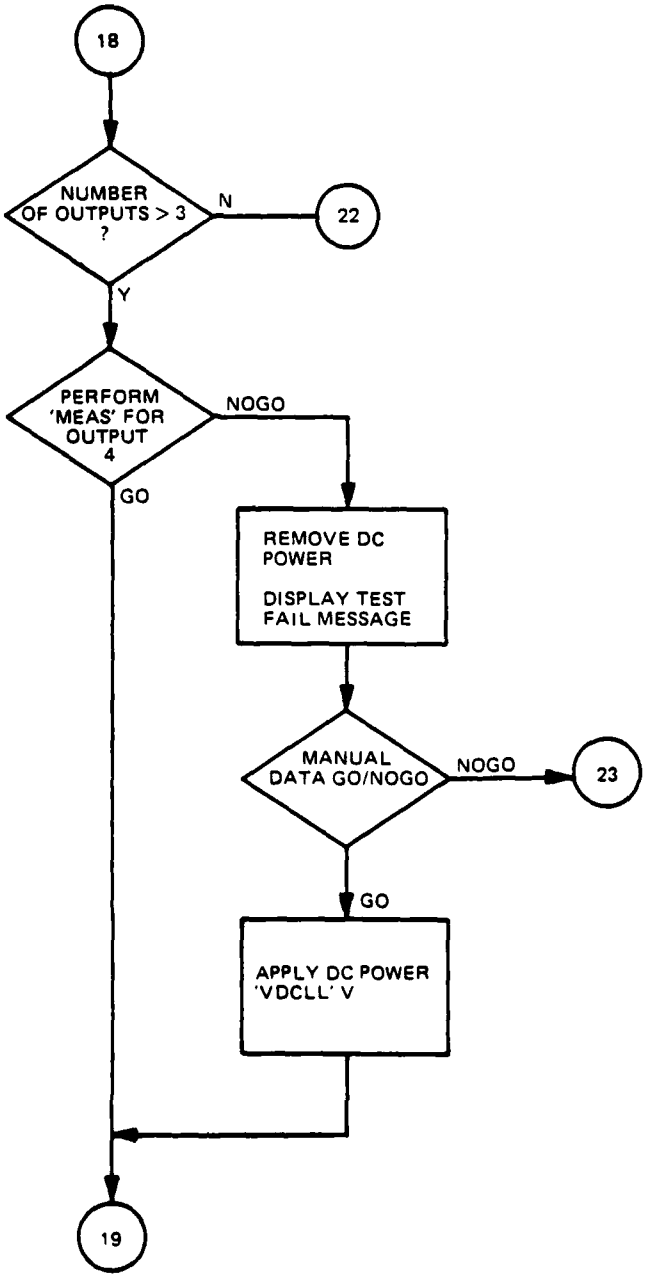

12
NUMBER OF O/P > 4 ?
N
15
Y
APPLY DC POWER 'VDCUL' V
PERFORM 'MEAS' FOR OUTPUT 5
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCUL'
13

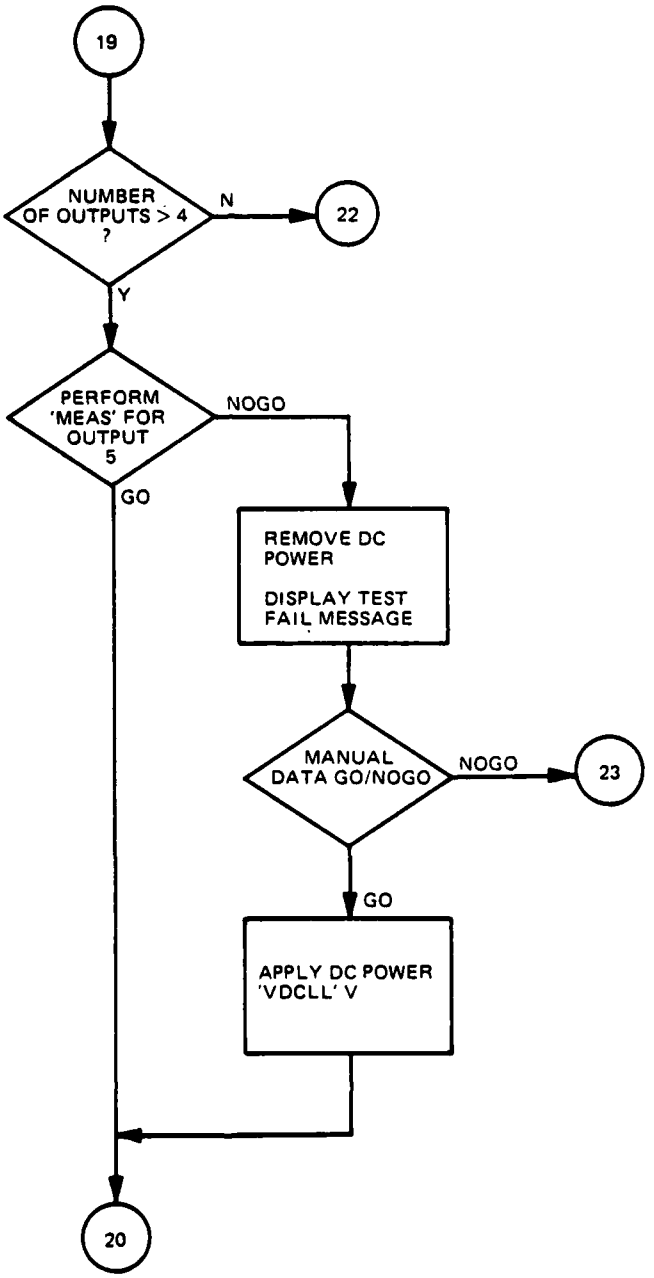

13
NUMBER OF O/P > 5 ?
N
15
Y
APPLY DC POWER 'VDCUL' V
PERFORM 'MEAS' FOR OUTPUT 6
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCUL'
14

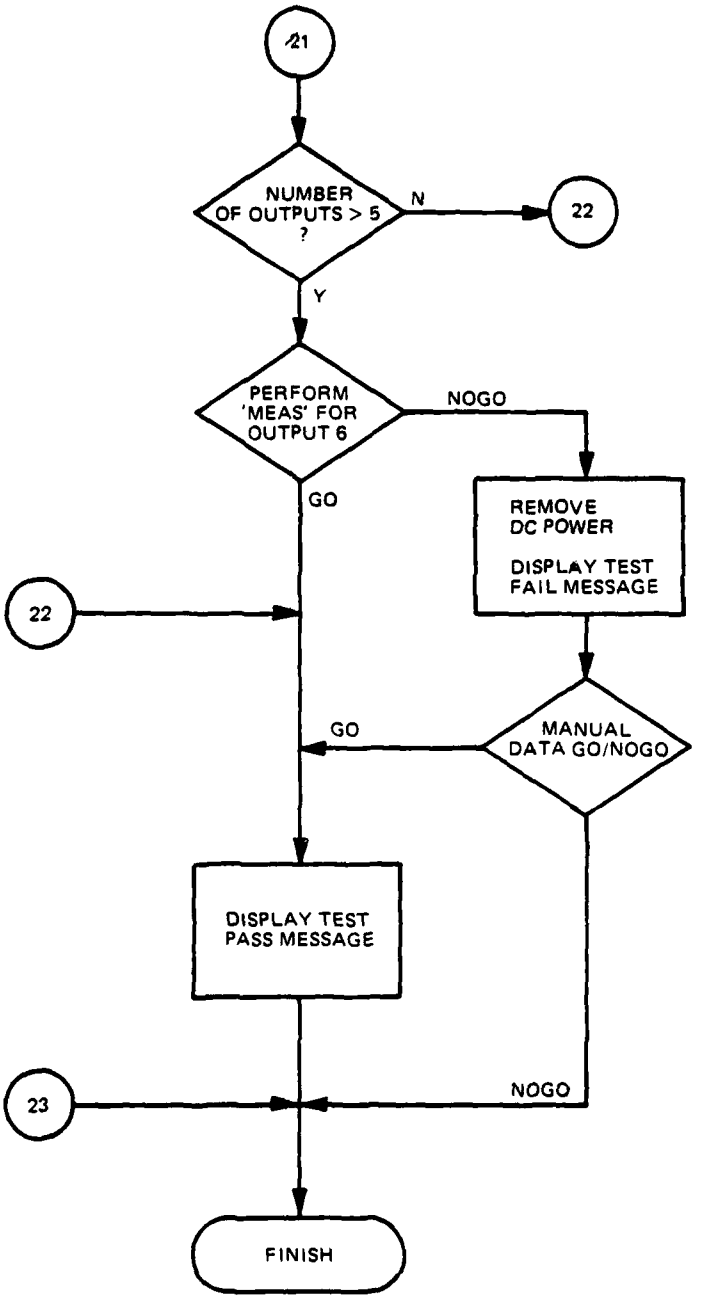

14
15
APPLY DC POWER 'VDCLL' V
PERFORM 'MEAS' FOR OUTPUT 1
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCLL'
16


16
NUMBER OF OUTPUTS > 1 ?
N
22
Y
PERFORM 'MEAS' FOR OUTPUT 2
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCLL' V
17

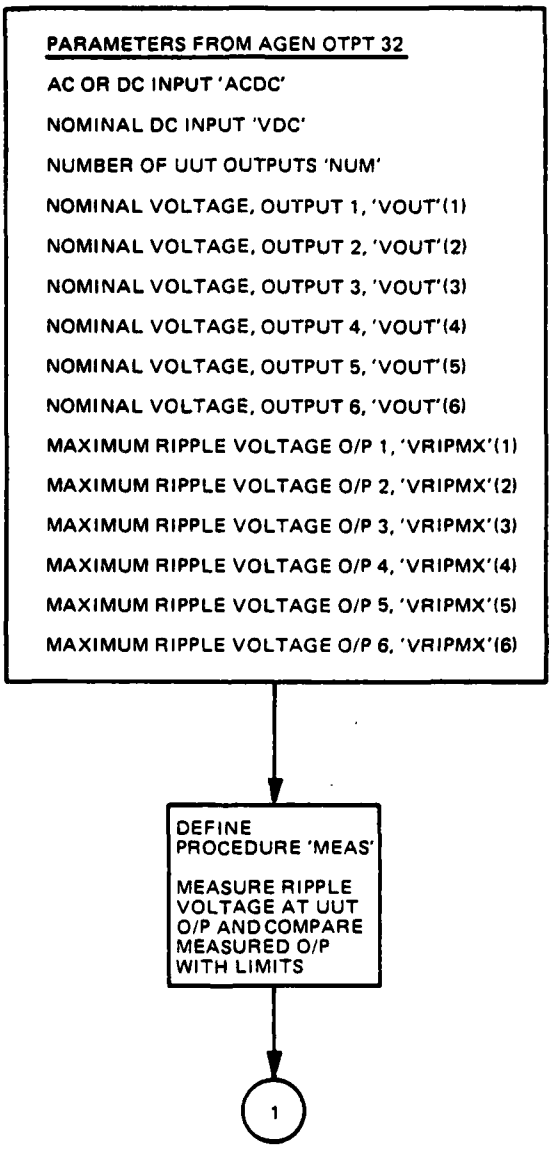

17
NUMBER OF OUTPUTS > 2 ?
N
22
Y
PERFORM 'MEAS' FOR OUTPUT 3
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCLL' V
18

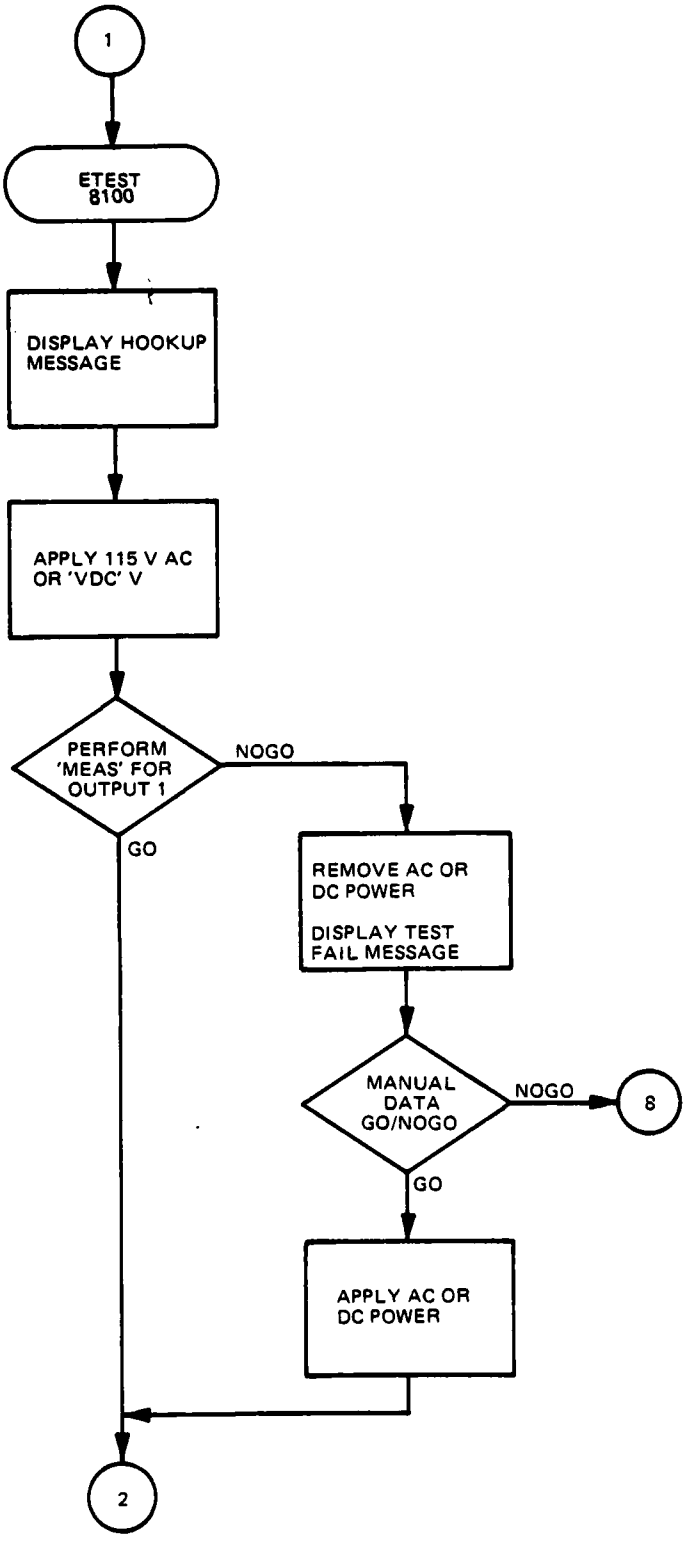

18
NUMBER OF OUTPUTS > 3 ?
N
22
Y
PERFORM 'MEAS' FOR OUTPUT 4
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCLL' V
19

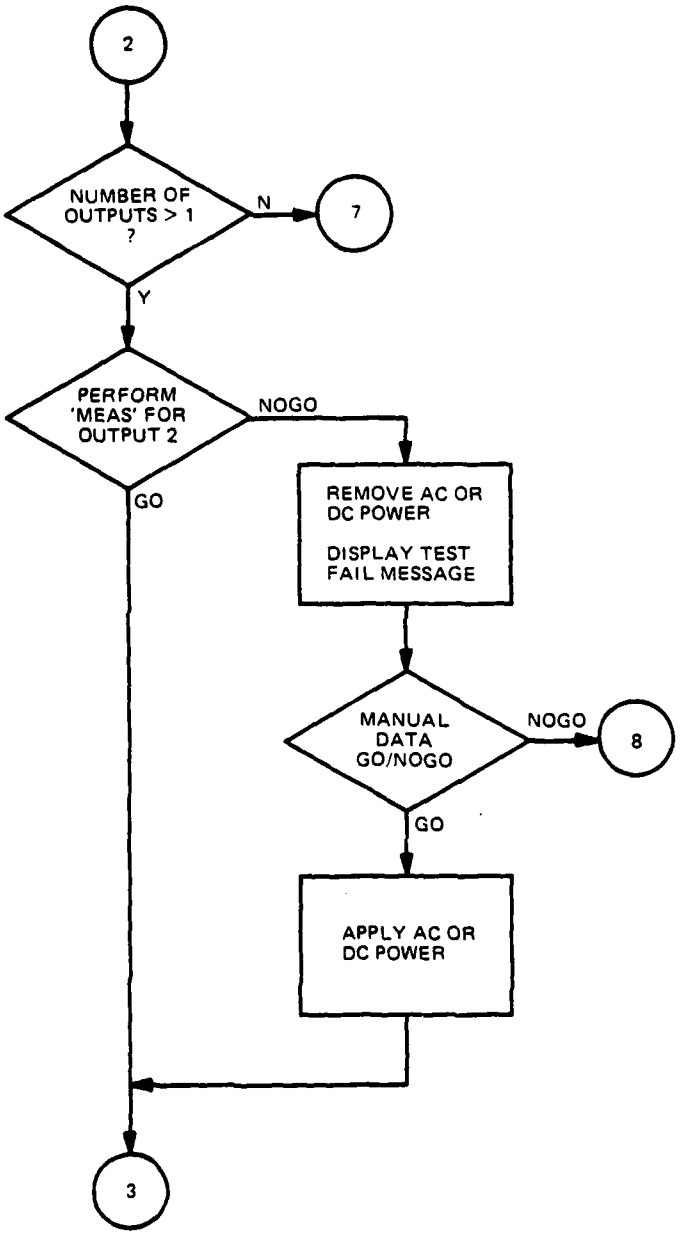

19
NUMBER OF OUTPUTS > 4 ?
N
22
Y
PERFORM 'MEAS' FOR OUTPUT 5
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
23
GO
APPLY DC POWER 'VDCLL' V
20

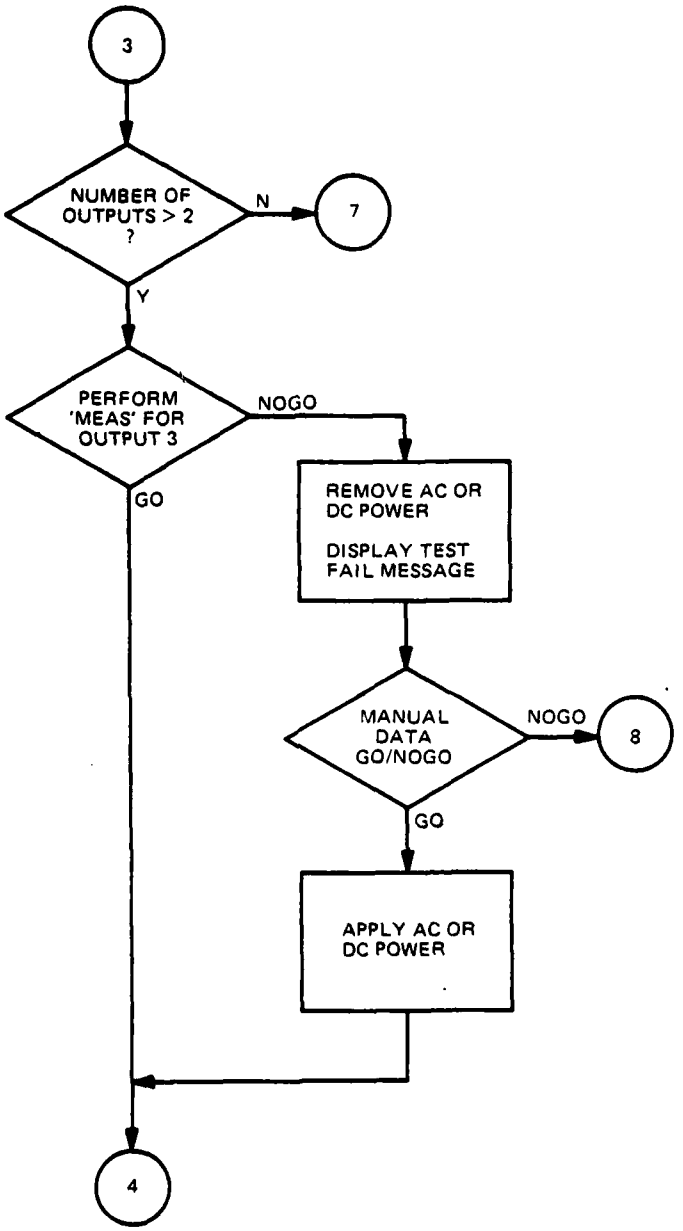

21
NUMBER OF OUTPUTS > 5 ?
N
22
Y
PERFORM 'MEAS' FOR OUTPUT 6
NOGO
GO
REMOVE DC POWER
DISPLAY TEST FAIL MESSAGE
22
GO
MANUAL DATA GO/NOGO
DISPLAY TEST PASS MESSAGE
23
NOGO
FINISH

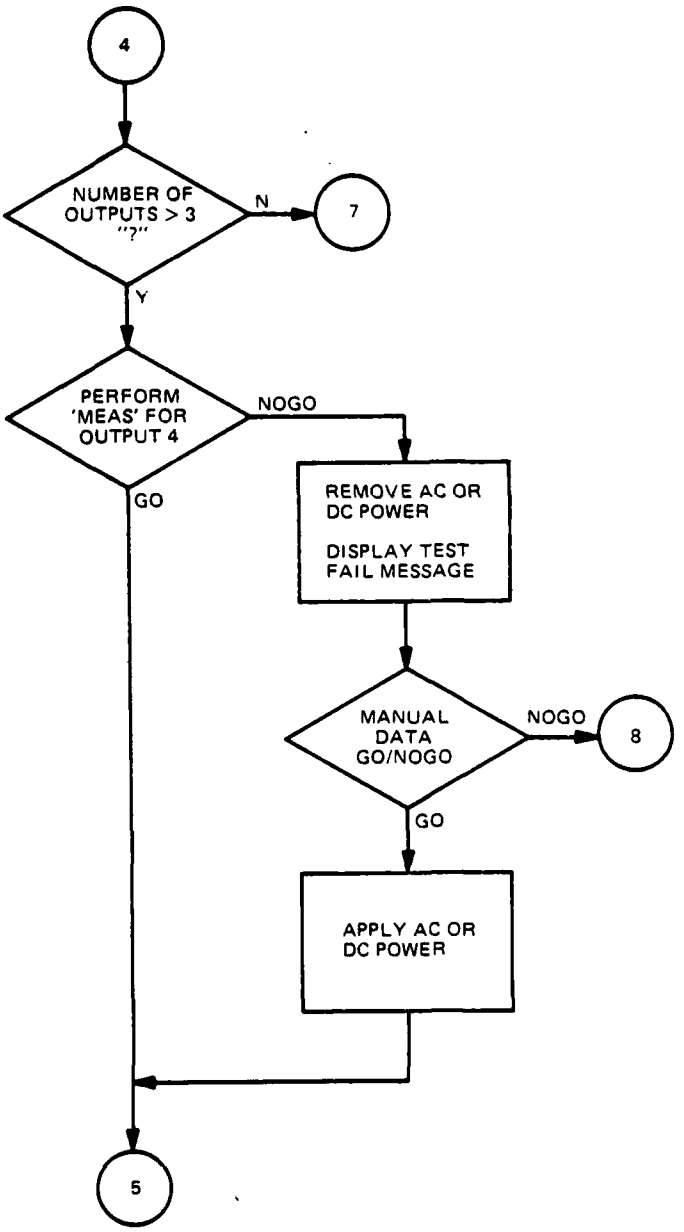
3.6 Power Supply Ripple Test Flow Chart

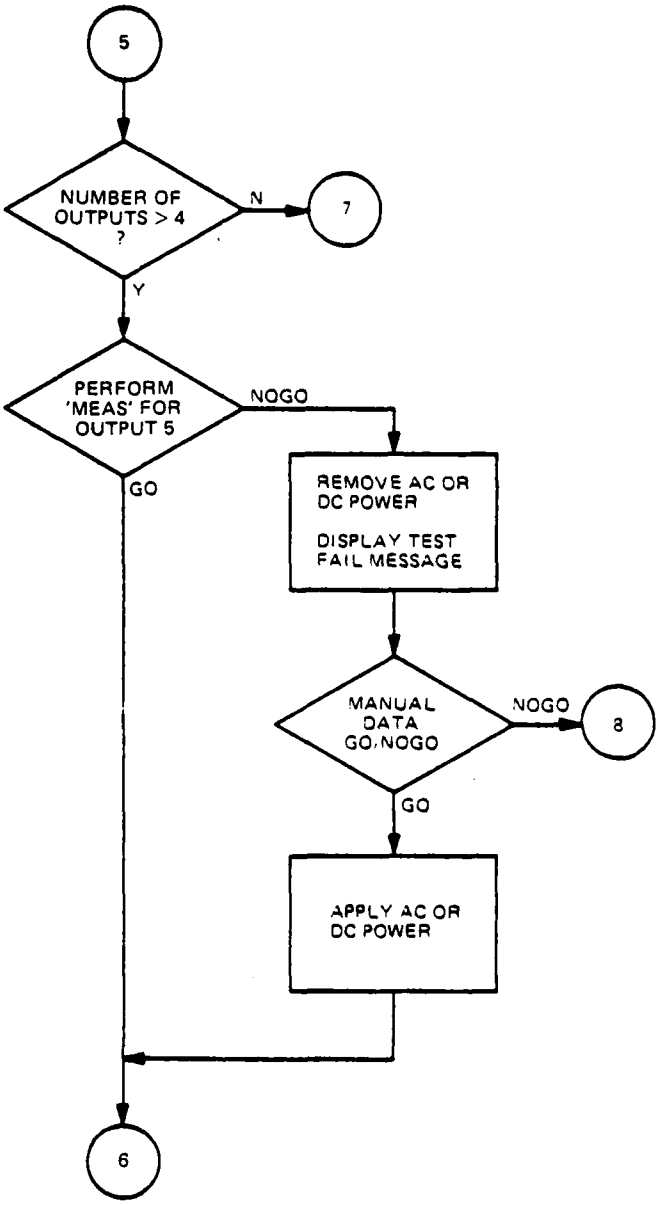


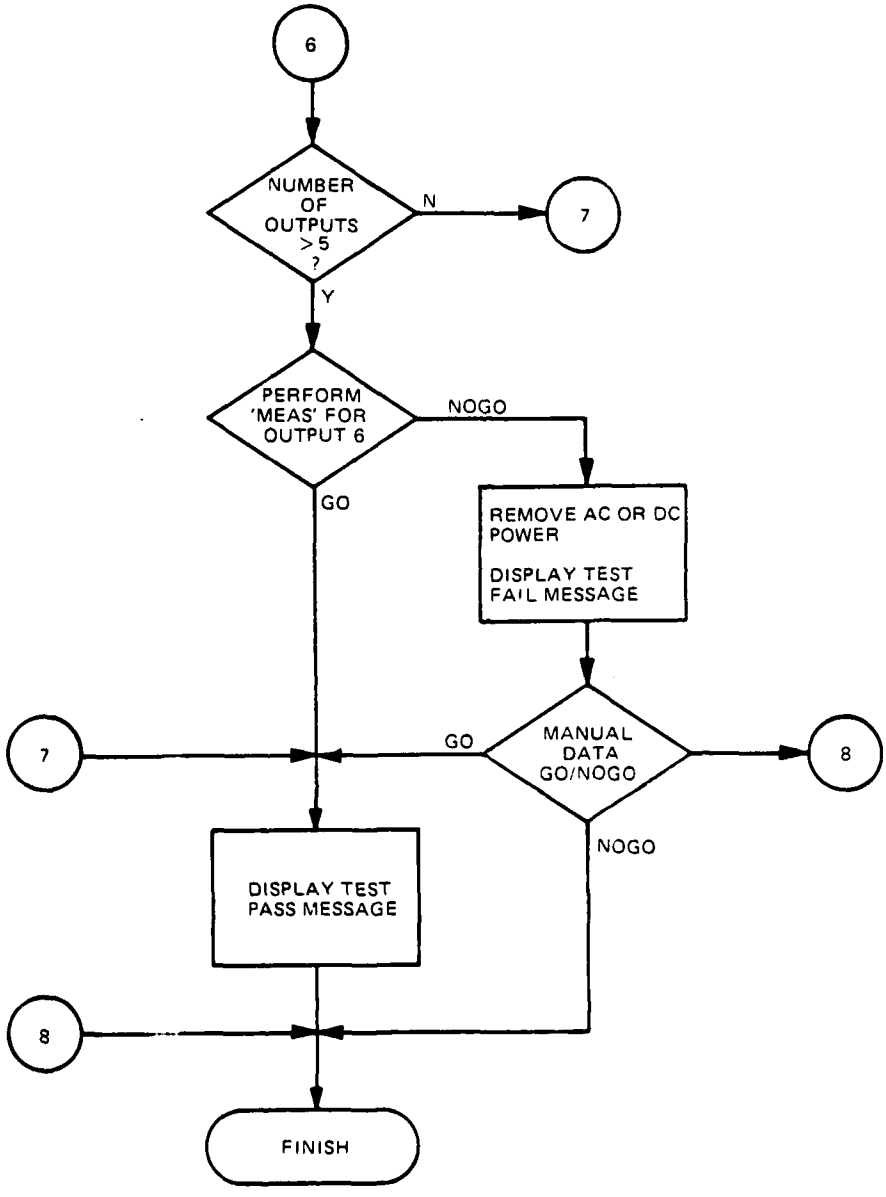

1
ETEST 8100
DISPLAY HOOKUP MESSAGE
APPLY 115 V AC OR 'VDC' V
PERFORM 'MEAS' FOR OUTPUT 1
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
2


2
NUMBER OF OUTPUTS > 1 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 2
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
3

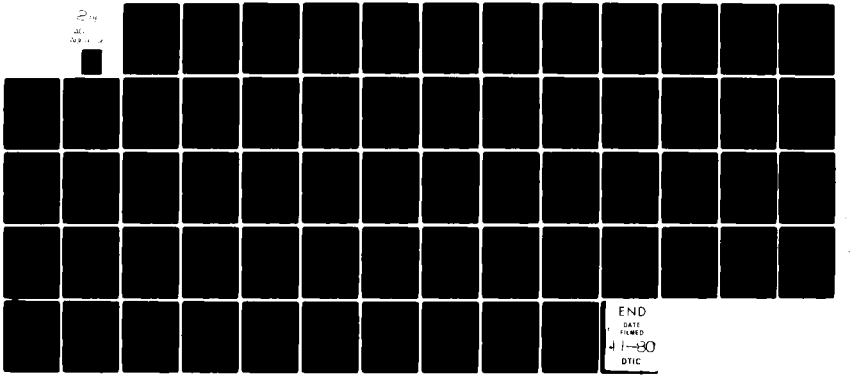

3
NUMBER OF OUTPUTS > 2 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 3
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
4


4
NUMBER OF OUTPUTS > 3 "?"
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 4
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
5

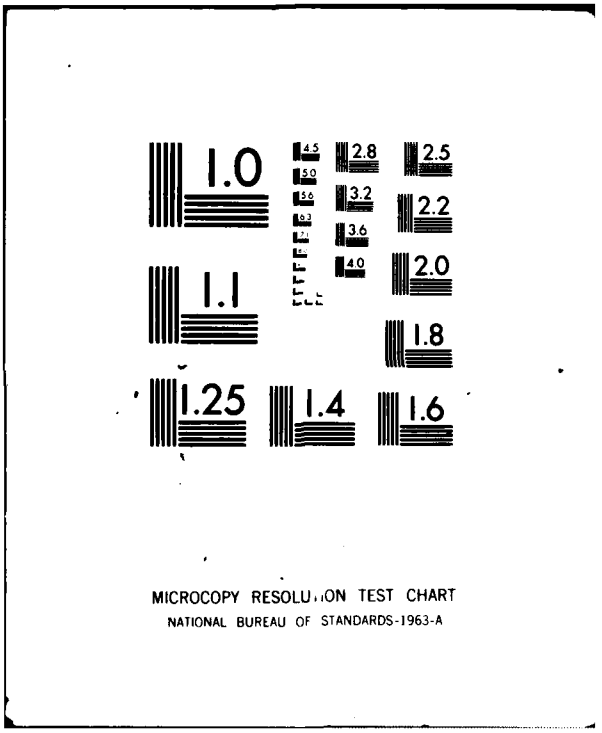

5
NUMBER OF OUTPUTS > 4 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 5
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
6


6
NUMBER OF OUTPUTS >5 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 6
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
7
GO
MANUAL DATA GO/NOGO
8
NOGO
DISPLAY TEST PASS MESSAGE
8
FINISH

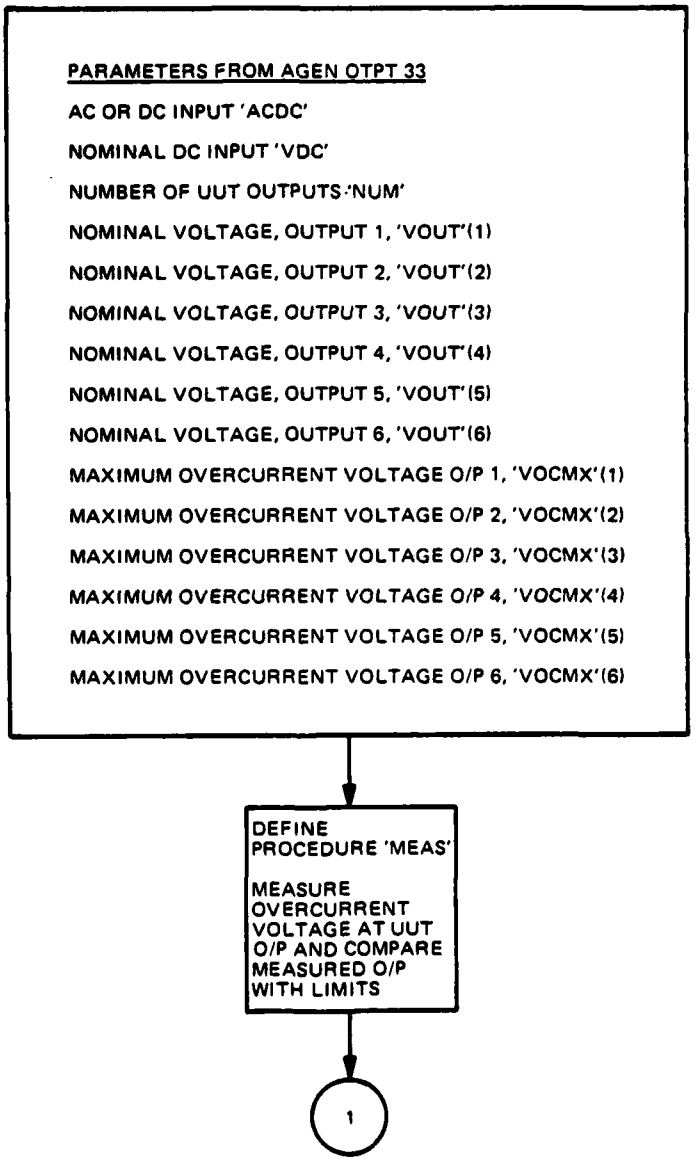
AD-A089 796 HARRIS CORP SYOSSET NY PRD ELECTRONICS DIV F/G 9/2
ATLAS TEST PROGRAM GENERATOR II (AGEN II) USER'S GUIDE, VOLUME --ETC(U
AUG 80 J KUNG DAAB07-78-C-2015
UNCLASSIFIED CORADCOM-78-2015-F2 NL

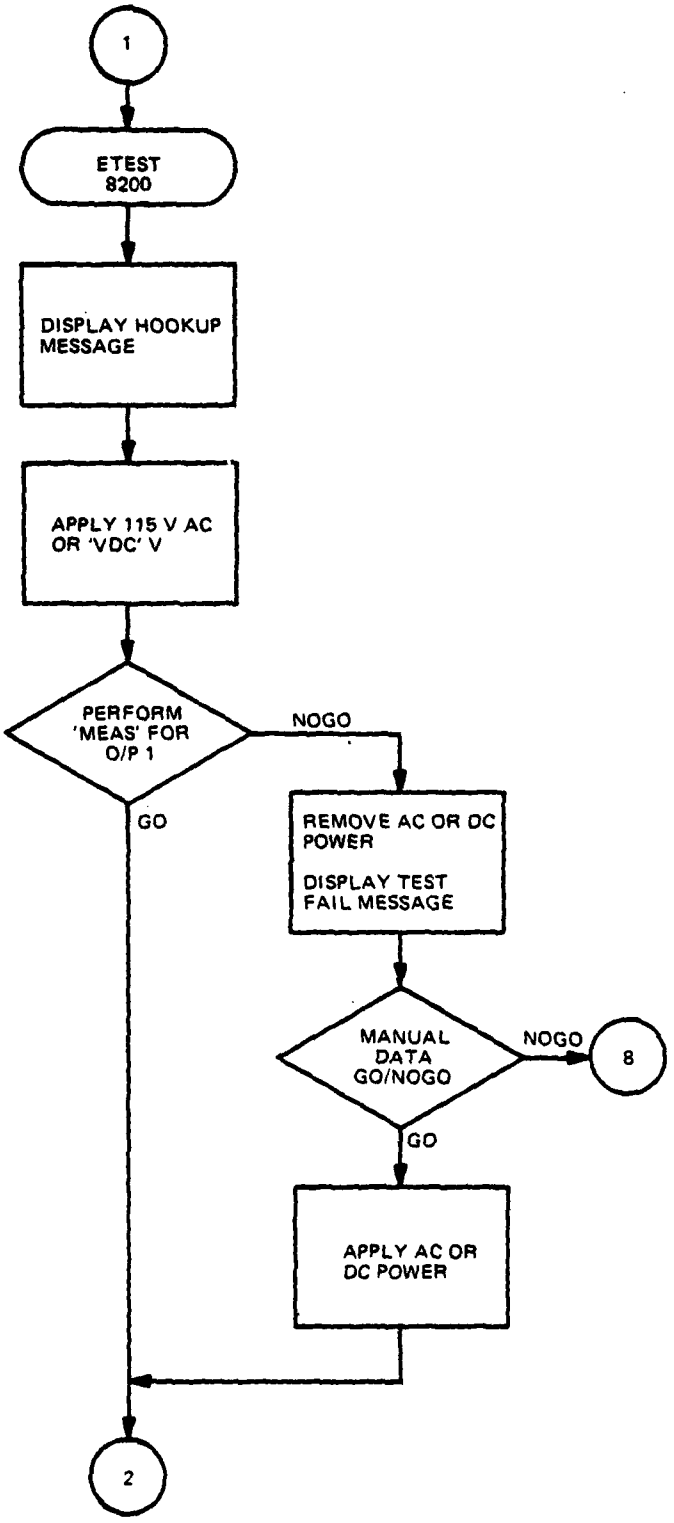


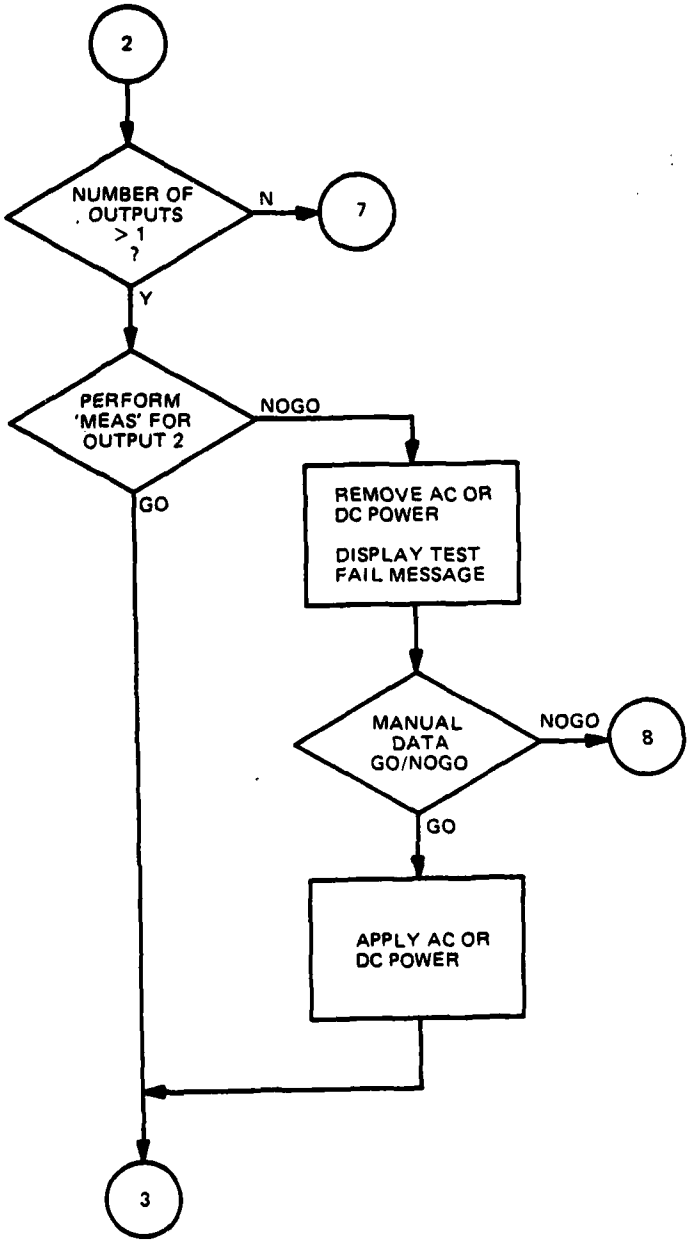
END
DATE FILMED
11-80
DTIC

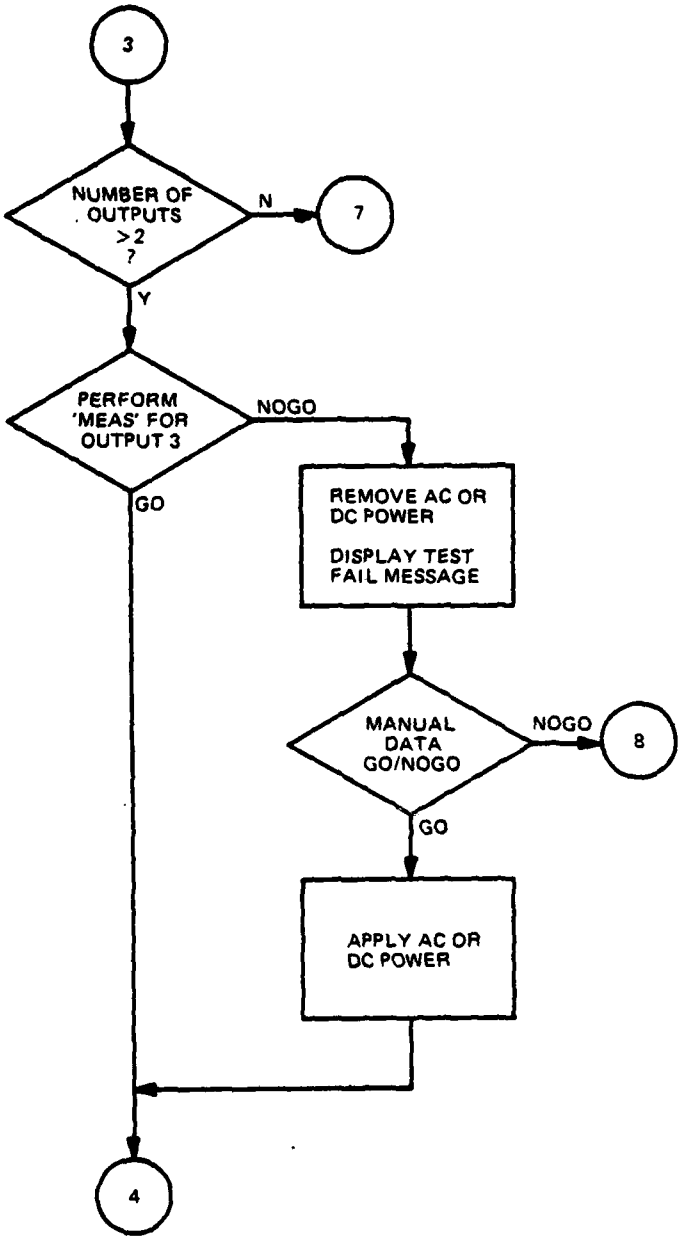

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
4.5
5.0
5.6
6.3
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

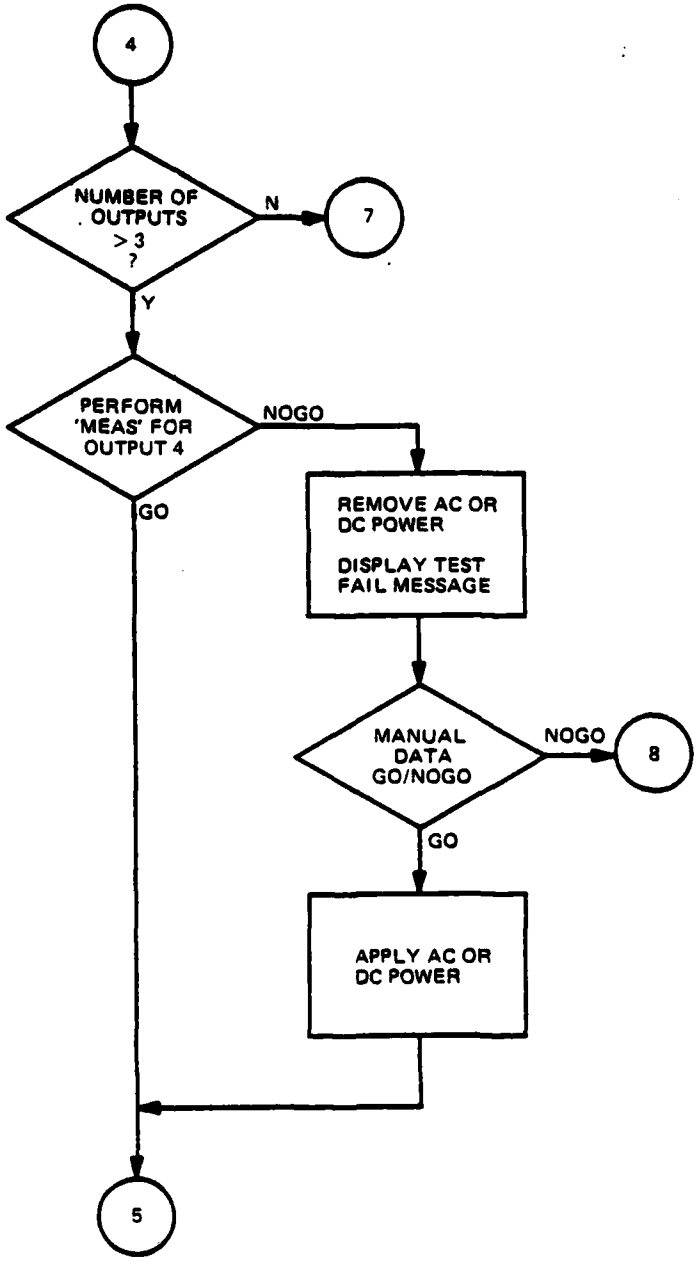
3.7 Power Supply Over Current Test Flow Chart

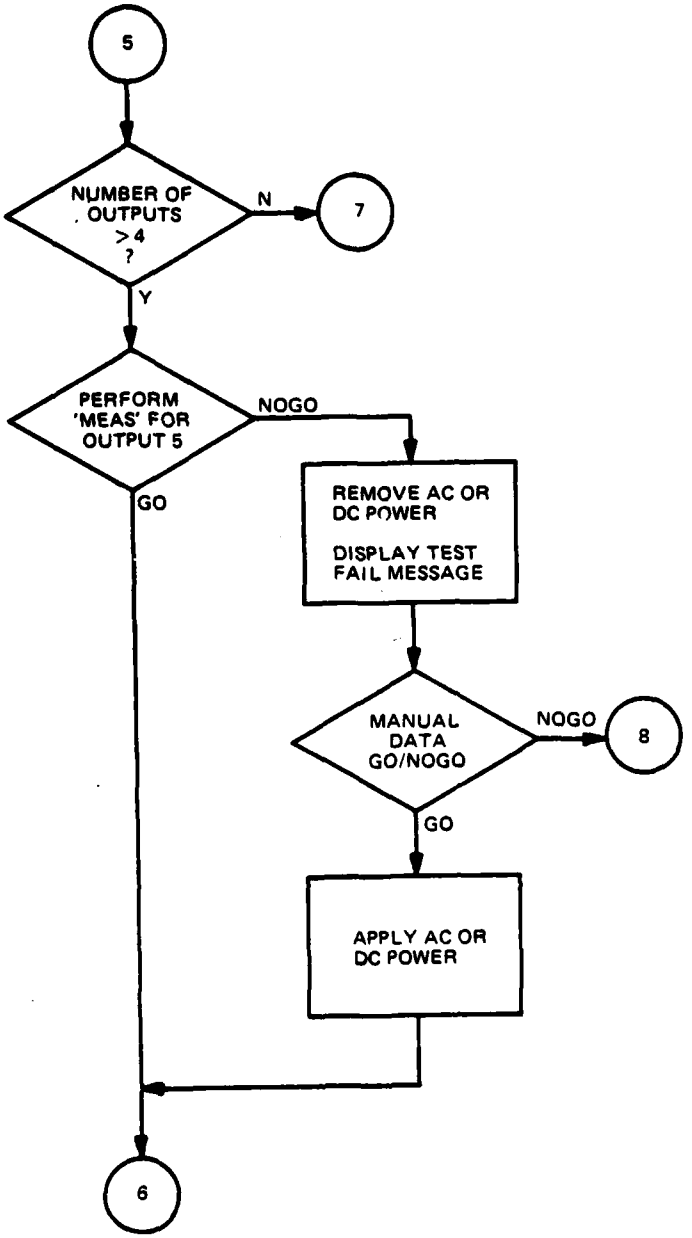


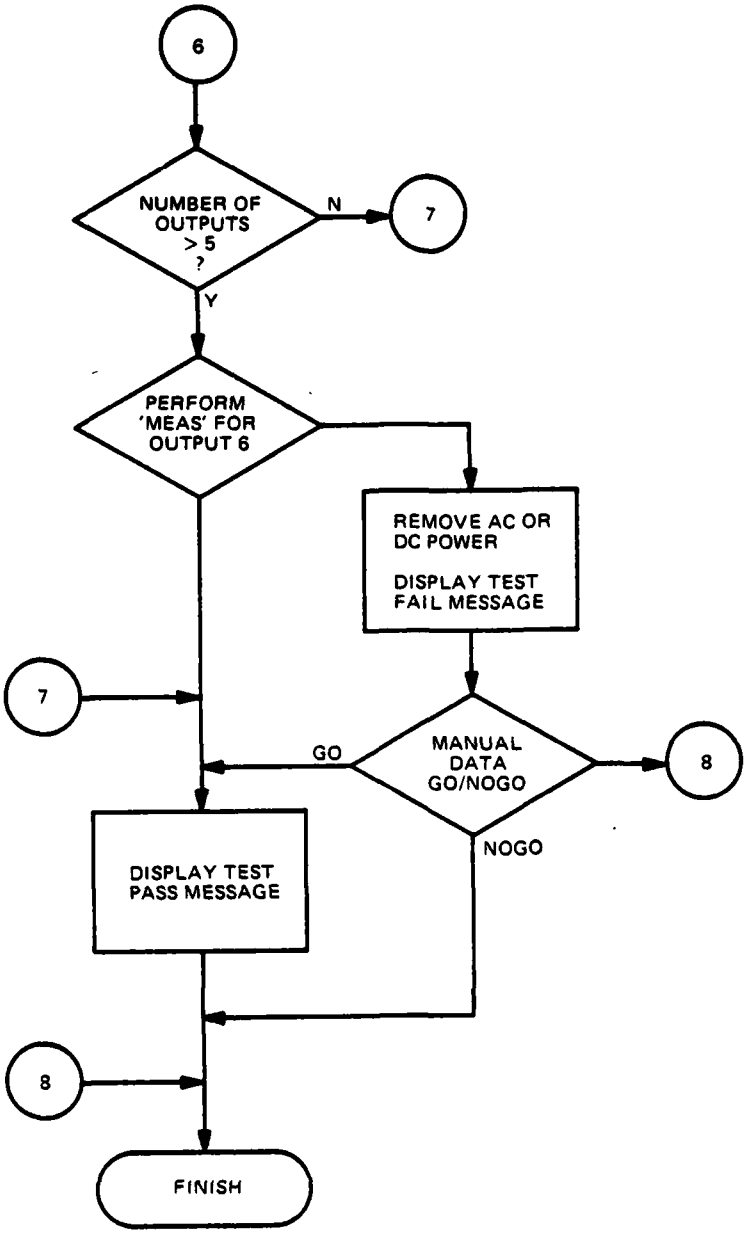

1
ETEST
8200
DISPLAY HOOKUP
MESSAGE
APPLY 115 V AC
OR 'VDC' V
PERFORM
'MEAS' FOR
O/P 1
NOGO
GO
REMOVE AC OR DC
POWER
DISPLAY TEST
FAIL MESSAGE
MANUAL
DATA
GO/NOGO
NOGO
8
GO
APPLY AC OR
DC POWER
2


2
NUMBER OF OUTPUTS > 1 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 2
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
3

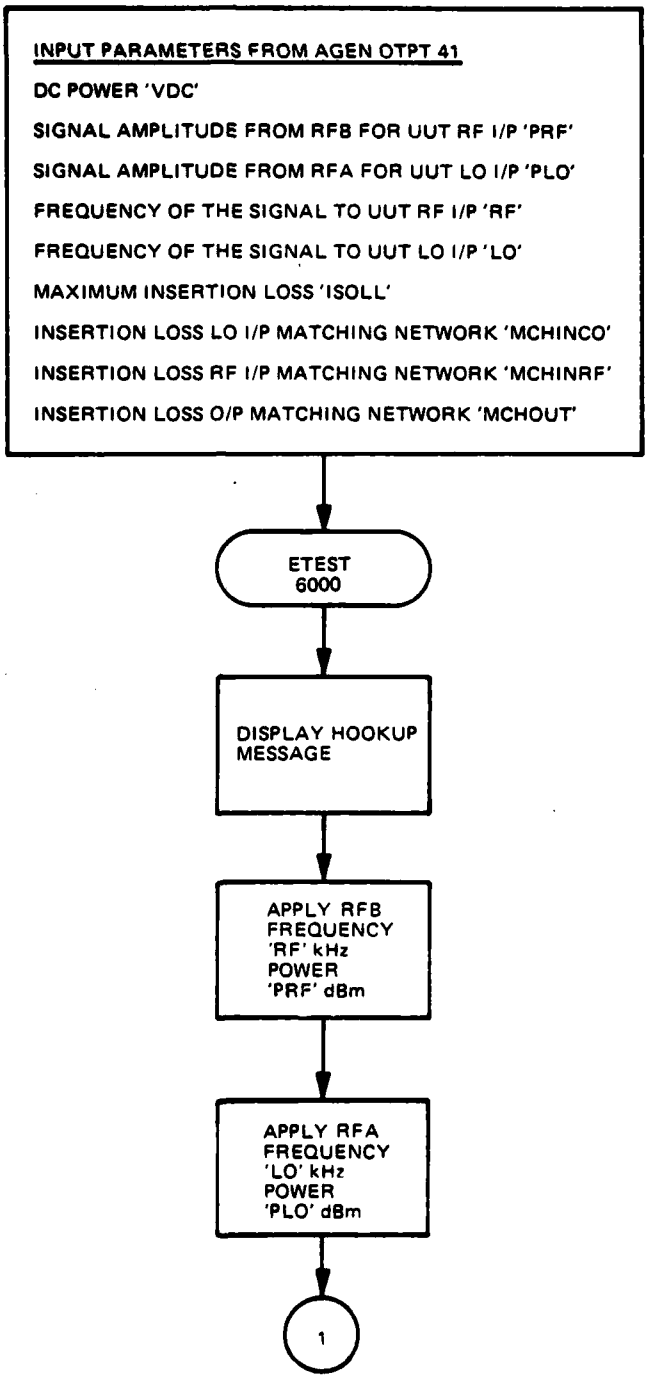

3
NUMBER OF OUTPUTS >2 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 3
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
4

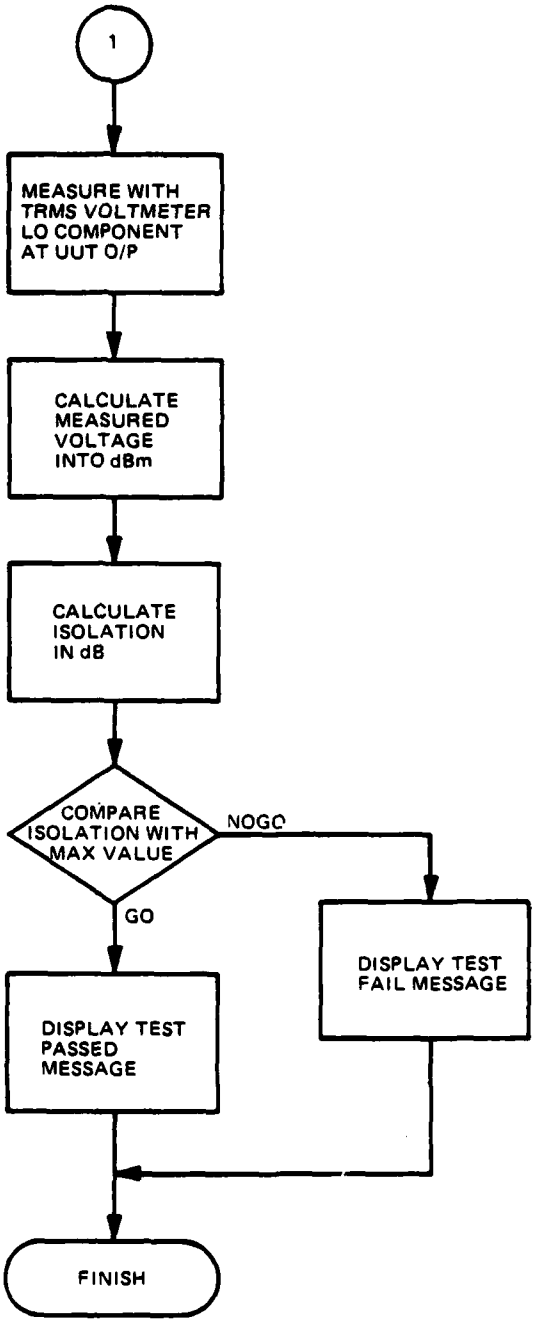

4
NUMBER OF OUTPUTS > 3 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 4
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
5


5
NUMBER OF OUTPUTS >4 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 5
NOGO
GO
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
MANUAL DATA GO/NOGO
NOGO
8
GO
APPLY AC OR DC POWER
6

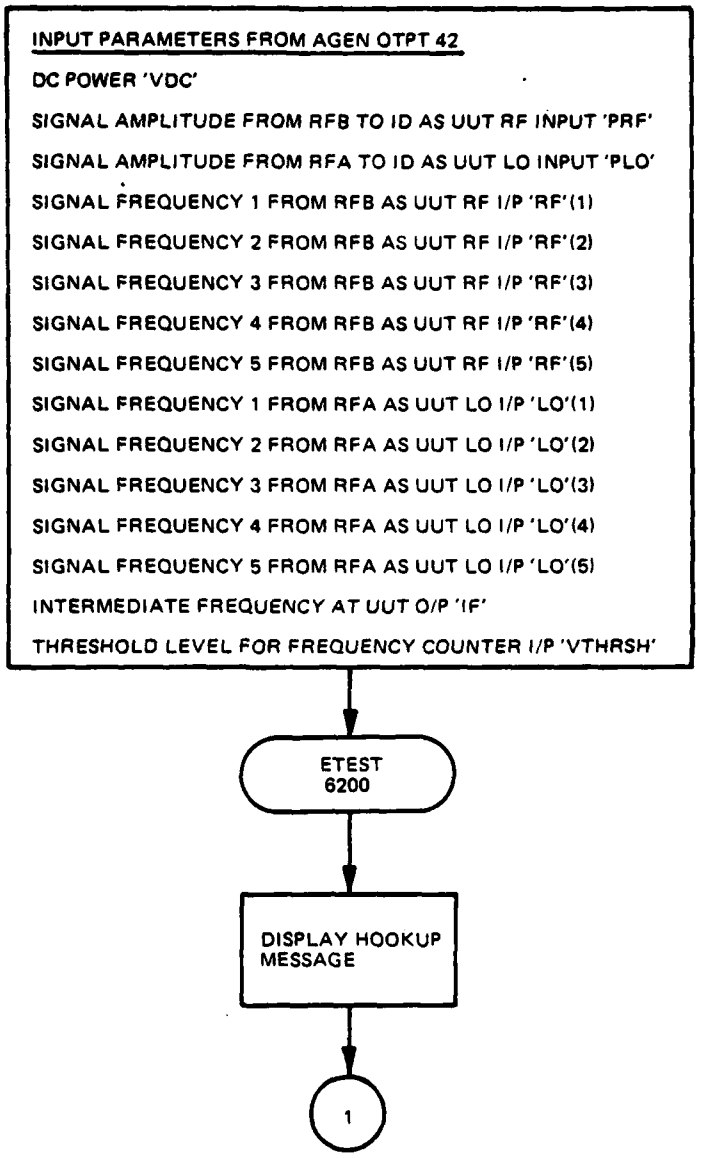

6
NUMBER OF OUTPUTS > 5 ?
N
7
Y
PERFORM 'MEAS' FOR OUTPUT 6
REMOVE AC OR DC POWER
DISPLAY TEST FAIL MESSAGE
7
GO
MANUAL DATA GO/NOGO
8
NOGO
DISPLAY TEST PASS MESSAGE
8
FINISH

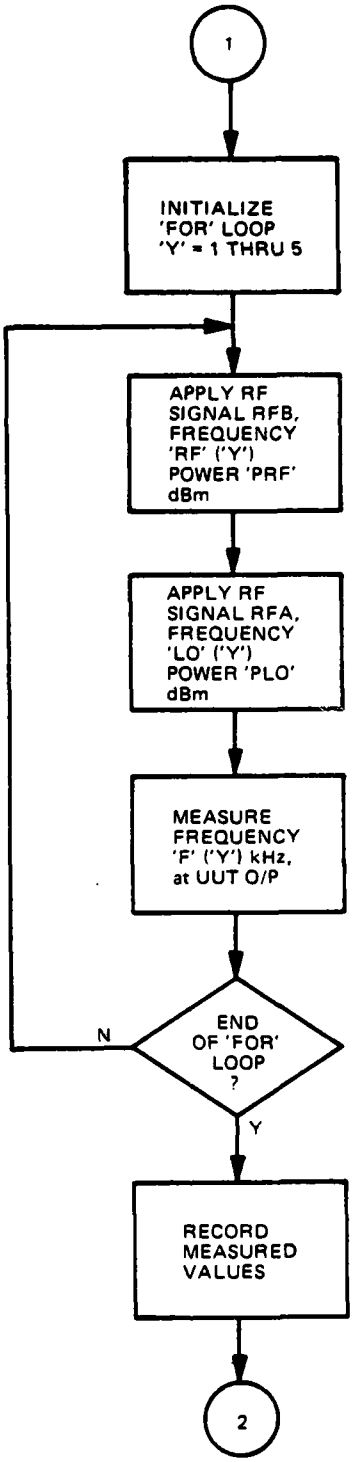
3.8 Mixer Isolation Test Flow Chart

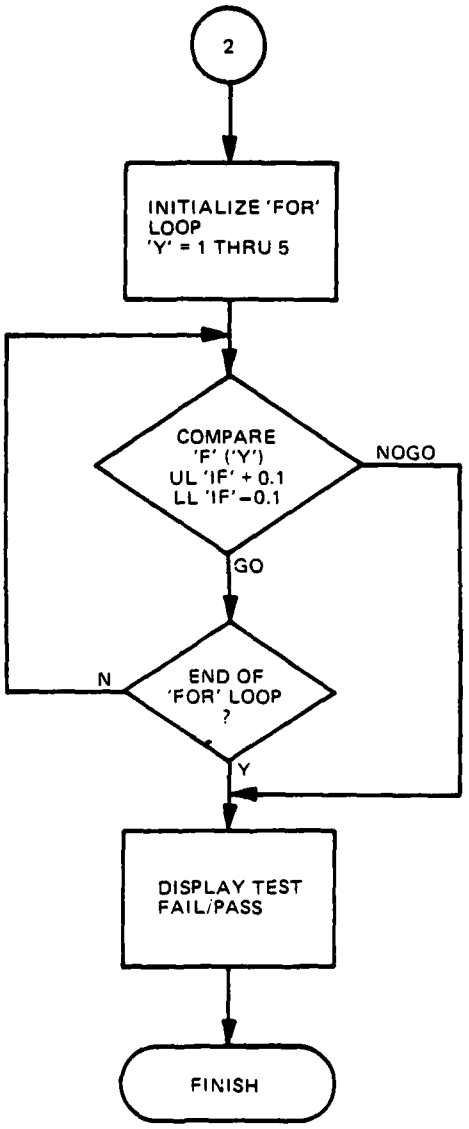



1
MEASURE WITH TRMS VOLTMETER LO COMPONENT AT UUT O/P
CALCULATE MEASURED VOLTAGE INTO dBm
CALCULATE ISOLATION IN dB
COMPARE ISOLATION WITH MAX VALUE
NOGO
GO
DISPLAY TEST FAIL MESSAGE
DISPLAY TEST PASSED MESSAGE
FINISH

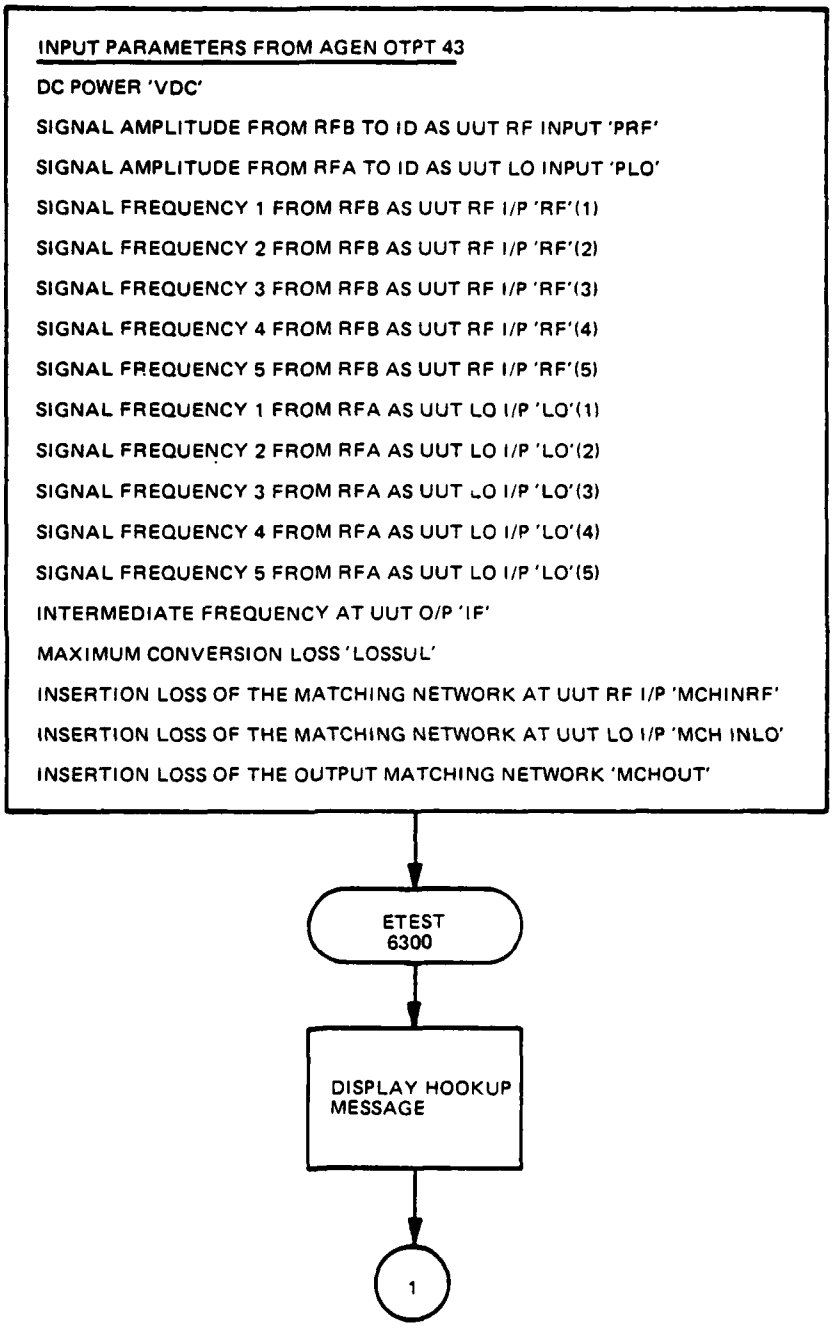
3.9 Mixer Frequency Response Test Flow Chart

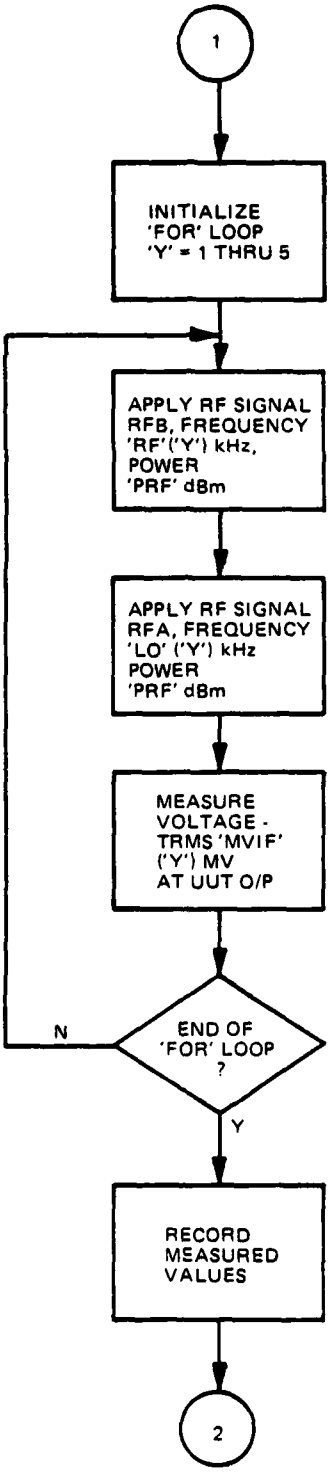


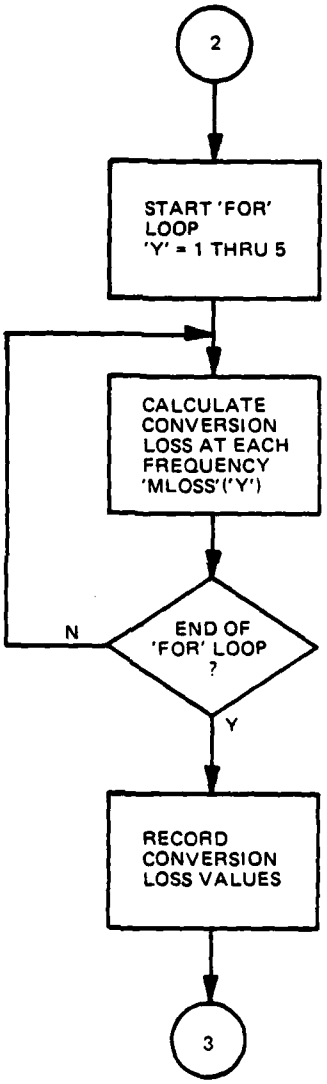

1
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
APPLY RF SIGNAL RFB, FREQUENCY 'RF' ('Y') POWER 'PRF' dBm
APPLY RF SIGNAL RFA, FREQUENCY 'LO' ('Y') POWER 'PLO' dBm
MEASURE FREQUENCY 'F' ('Y') kHz, at UUT O/P
END OF 'FOR' LOOP ?
N
Y
RECORD MEASURED VALUES
2

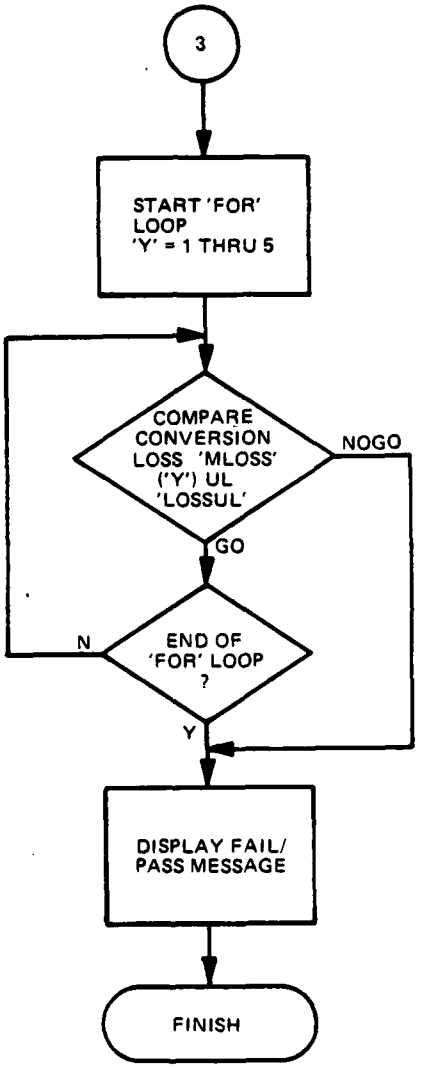

2
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
COMPARE 'F' ('Y') UL 'IF' + 0.1 LL 'IF' −0.1
NOGO
GO
N
END OF 'FOR' LOOP ?
Y
DISPLAY TEST FAIL/PASS
FINISH

3.10 Mixer Conversion Loss Test Flow Chart

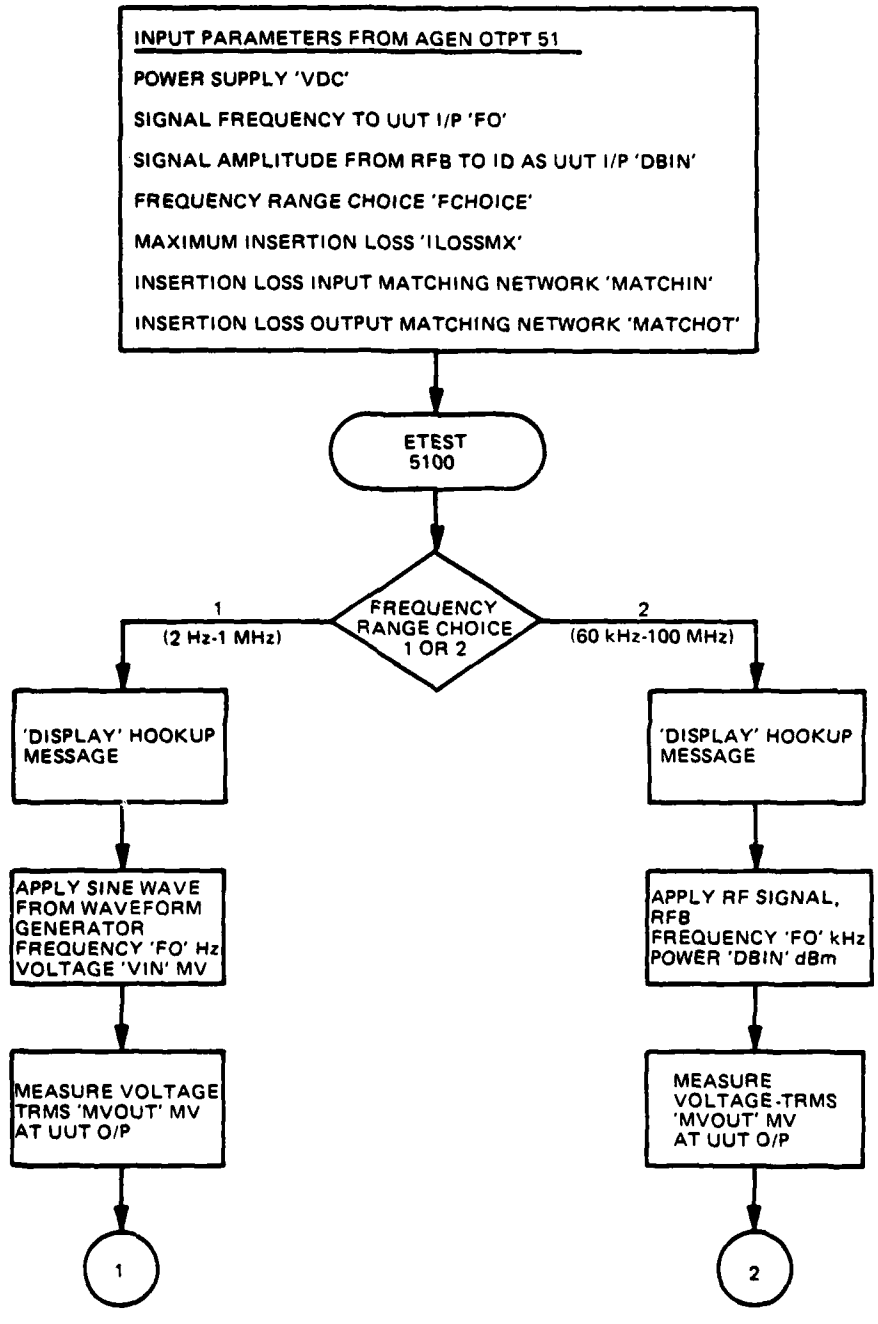


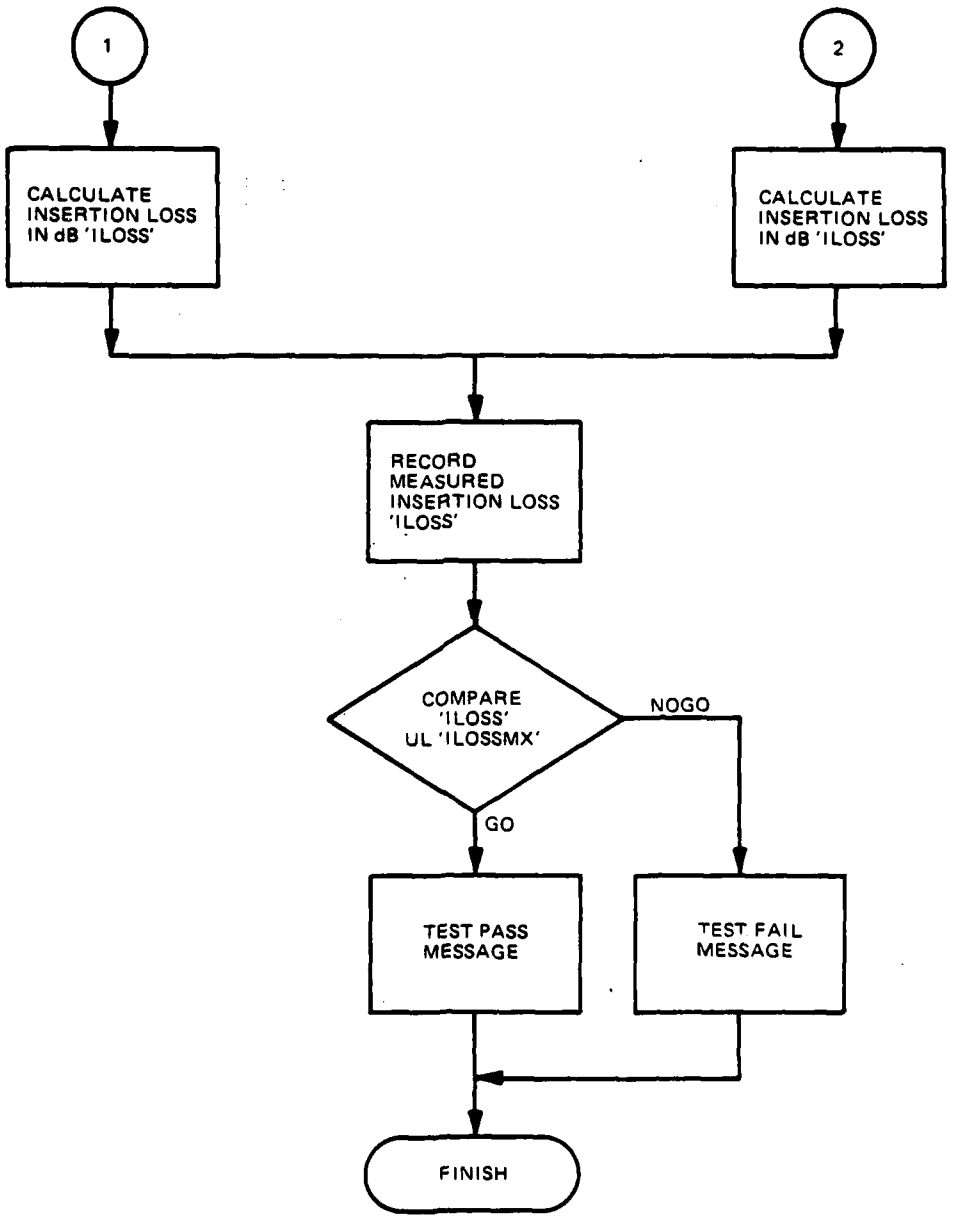

1
INITIALIZE 'FOR' LOOP 'Y' = 1 THRU 5
APPLY RF SIGNAL RFB, FREQUENCY 'RF' ('Y') kHz, POWER 'PRF' dBm
APPLY RF SIGNAL RFA, FREQUENCY 'LO' ('Y') kHz POWER 'PRF' dBm
MEASURE VOLTAGE - TRMS 'MVIF' ('Y') MV AT UUT O/P
END OF 'FOR' LOOP ?
N
Y
RECORD MEASURED VALUES
2


2
START 'FOR' LOOP 'Y' = 1 THRU 5
CALCULATE CONVERSION LOSS AT EACH FREQUENCY 'MLOSS'('Y')
END OF 'FOR' LOOP ?
N
Y
RECORD CONVERSION LOSS VALUES
3

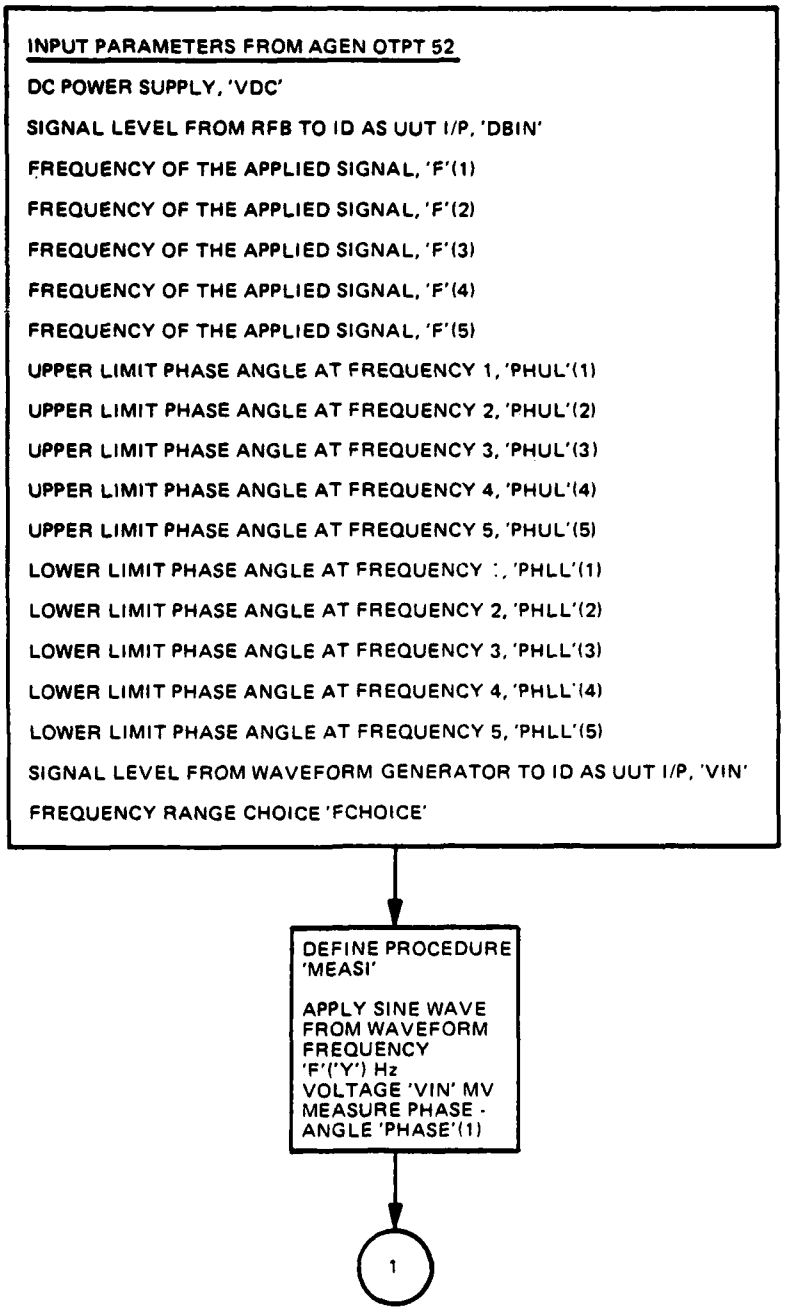

3
START 'FOR' LOOP 'Y' = 1 THRU 5
COMPARE CONVERSION LOSS 'MLOSS' ('Y') UL 'LOSSUL'
NOGO
GO
END OF 'FOR' LOOP ?
N
Y
DISPLAY FAIL/ PASS MESSAGE
FINISH

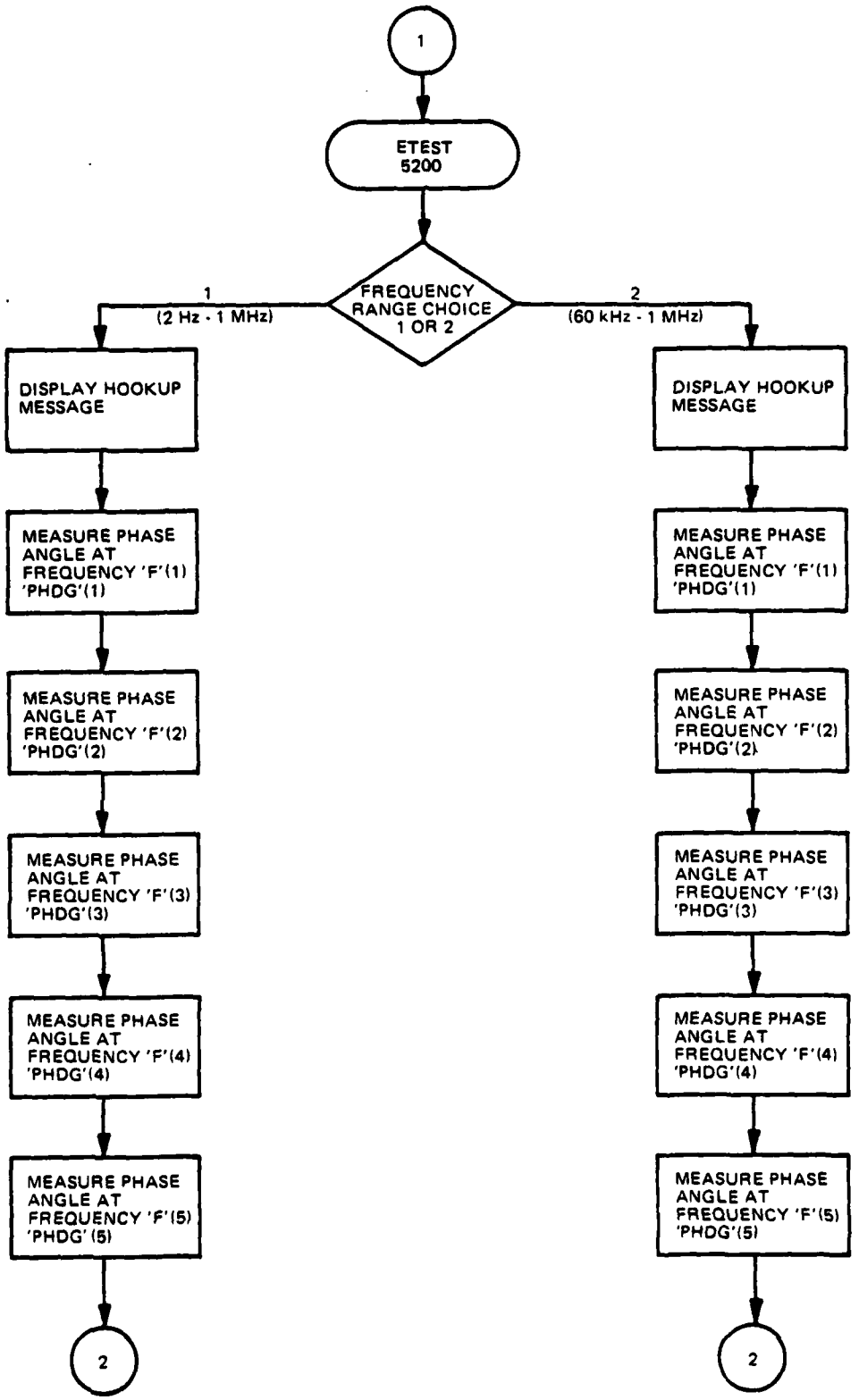
3.11 Filter Insertion Loss Test Flow Chart

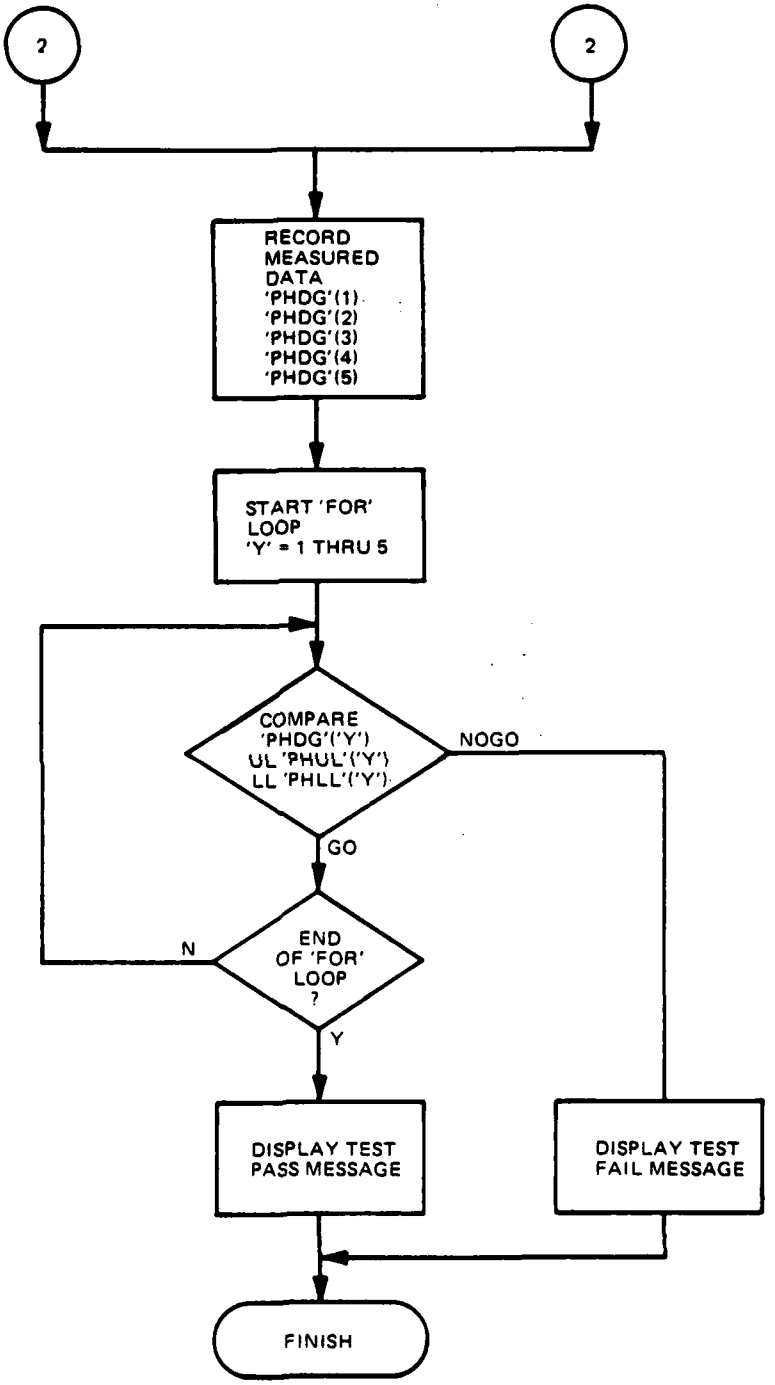



1
2
CALCULATE INSERTION LOSS IN dB 'ILOSS'
CALCULATE INSERTION LOSS IN dB 'ILOSS'
RECORD MEASURED INSERTION LOSS 'ILOSS'
COMPARE 'ILOSS' UL 'ILOSSMX'
NOGO
GO
TEST PASS MESSAGE
TEST FAIL MESSAGE
FINISH

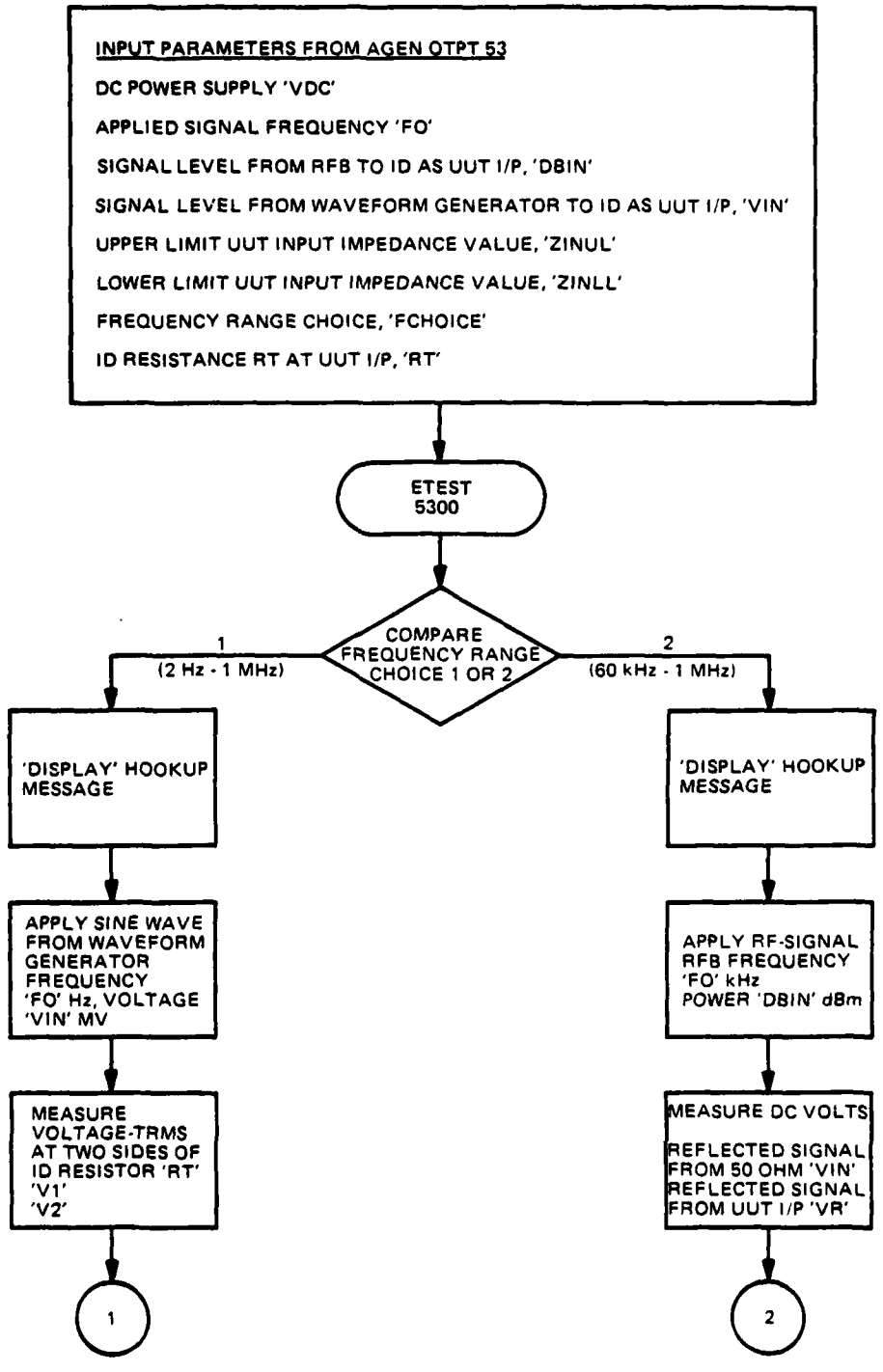
3.12 Filter Phase Response Test Flow Chart

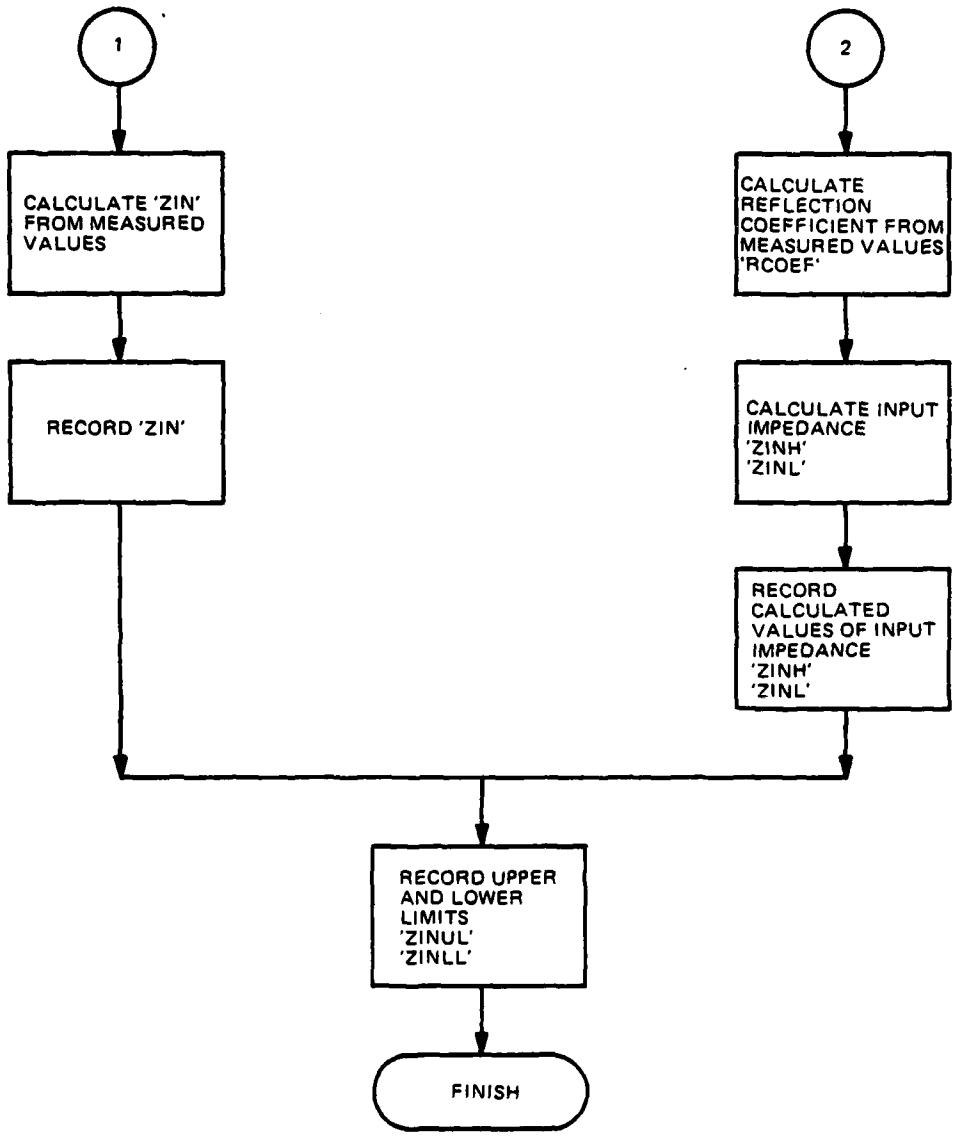



1
ETEST
5200
FREQUENCY
RANGE CHOICE
1 OR 2
1
(2 Hz - 1 MHz)
2
(60 kHz - 1 MHz)
DISPLAY HOOKUP
MESSAGE
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(1)
'PHDG'(1)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(2)
'PHDG'(2)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(3)
'PHDG'(3)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(4)
'PHDG'(4)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(5)
'PHDG'(5)
2
DISPLAY HOOKUP
MESSAGE
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(1)
'PHDG'(1)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(2)
'PHDG'(2)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(3)
'PHDG'(3)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(4)
'PHDG'(4)
MEASURE PHASE
ANGLE AT
FREQUENCY 'F'(5)
'PHDG'(5)
2

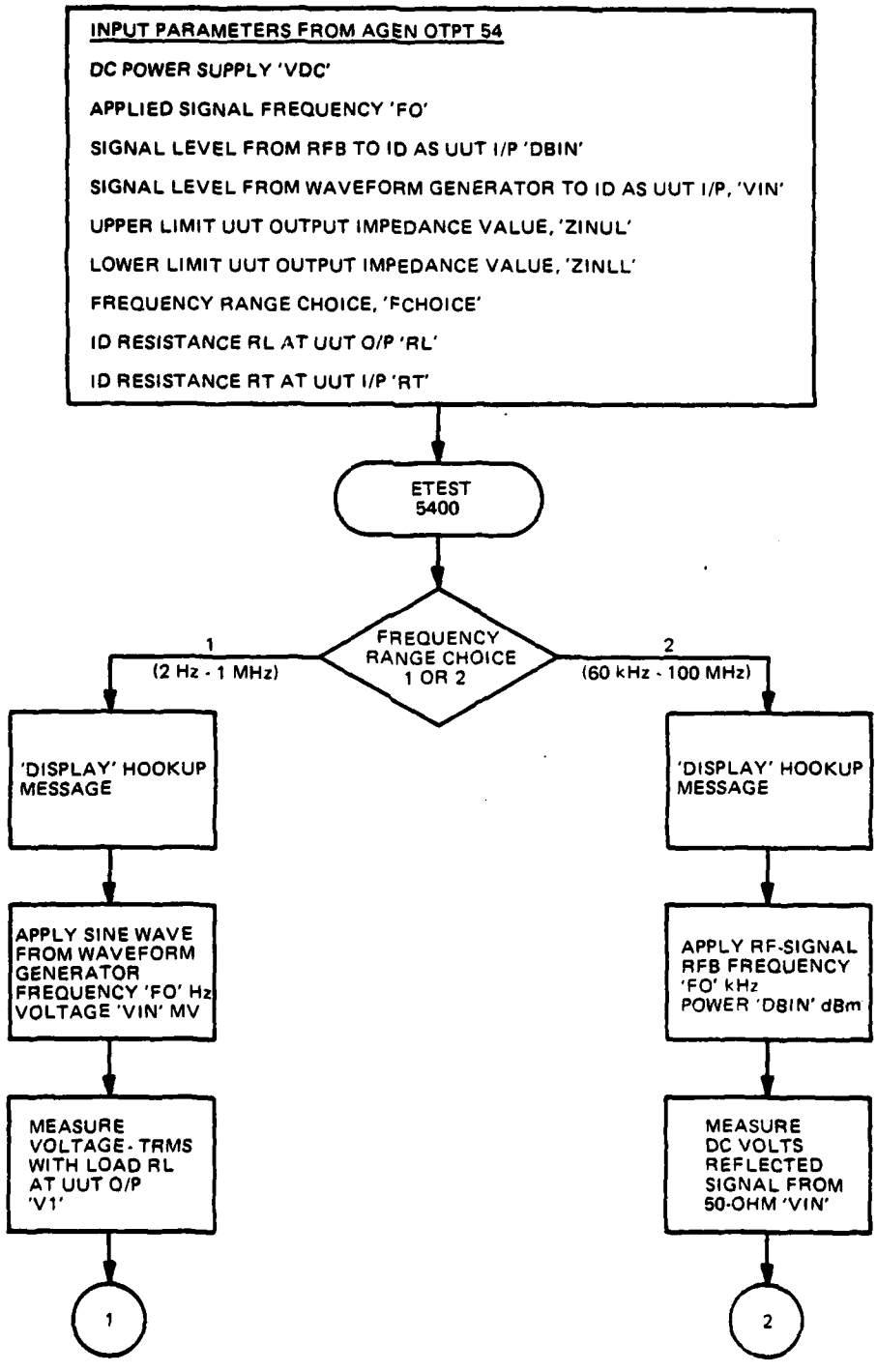

2
2
RECORD MEASURED DATA 'PHDG'(1) 'PHDG'(2) 'PHDG'(3) 'PHDG'(4) 'PHDG'(5)
START 'FOR' LOOP 'Y' = 1 THRU 5
COMPARE 'PHDG'('Y') UL 'PHUL'('Y') LL 'PHLL'('Y')
NOGO
GO
END OF 'FOR' LOOP ?
N
Y
DISPLAY TEST PASS MESSAGE
DISPLAY TEST FAIL MESSAGE
FINISH

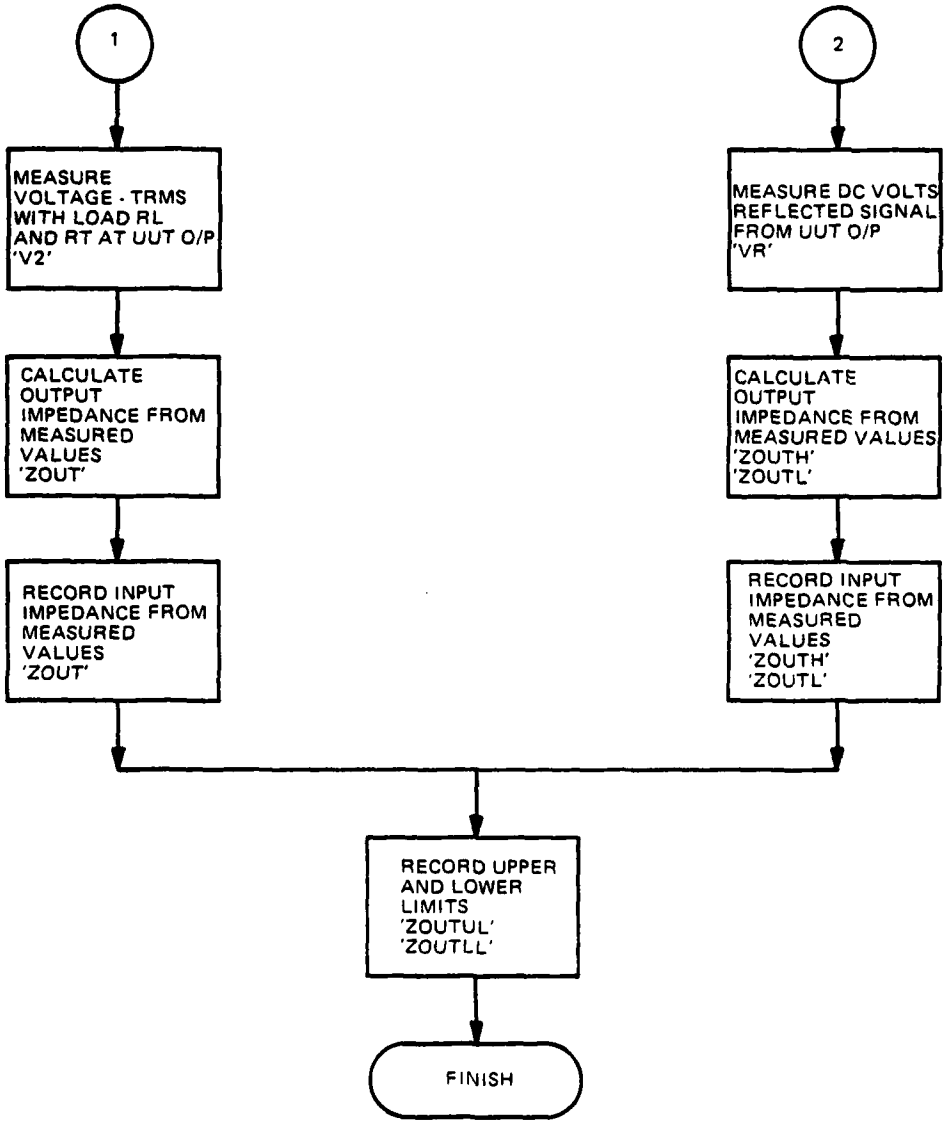
3.13 Filter Input Impedance Test Flow Chart



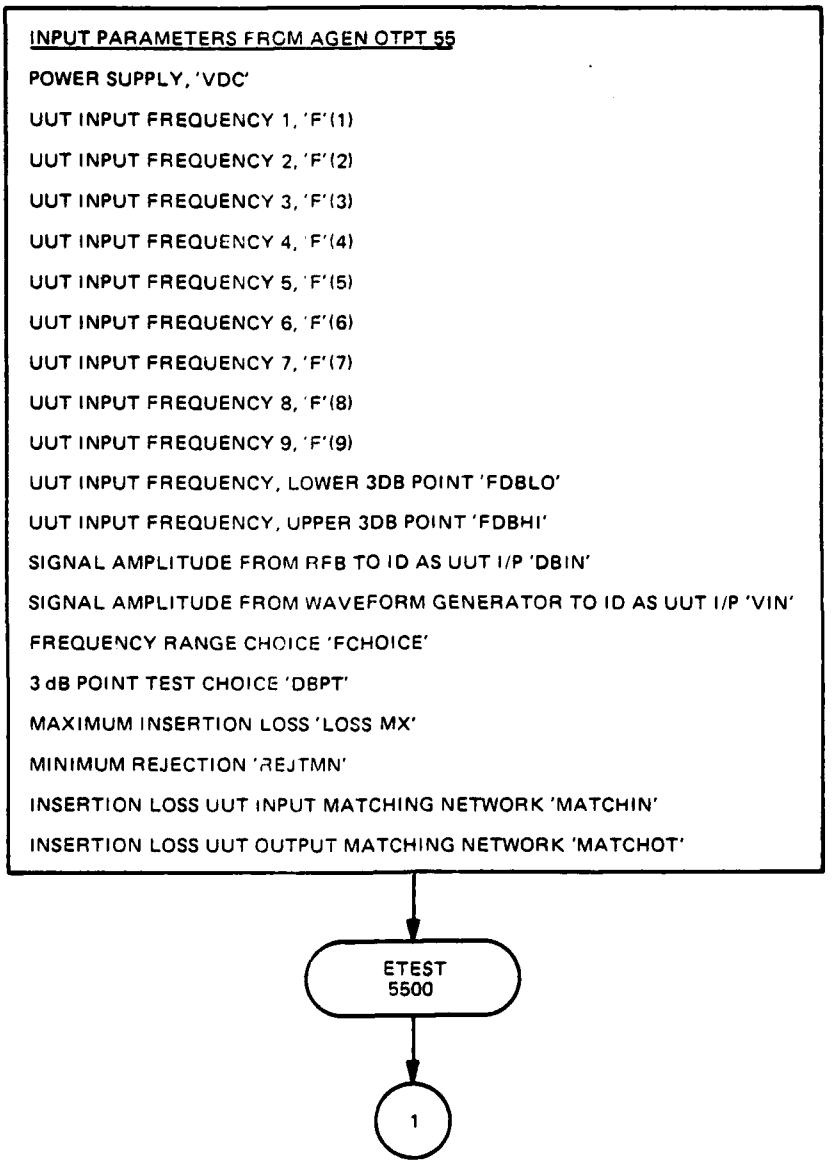

1
2
CALCULATE 'ZIN' FROM MEASURED VALUES
RECORD 'ZIN'
CALCULATE REFLECTION COEFFICIENT FROM MEASURED VALUES 'RCOEF'
CALCULATE INPUT IMPEDANCE 'ZINH' 'ZINL'
RECORD CALCULATED VALUES OF INPUT IMPEDANCE 'ZINH' 'ZINL'
RECORD UPPER AND LOWER LIMITS 'ZINUL' 'ZINLL'
FINISH

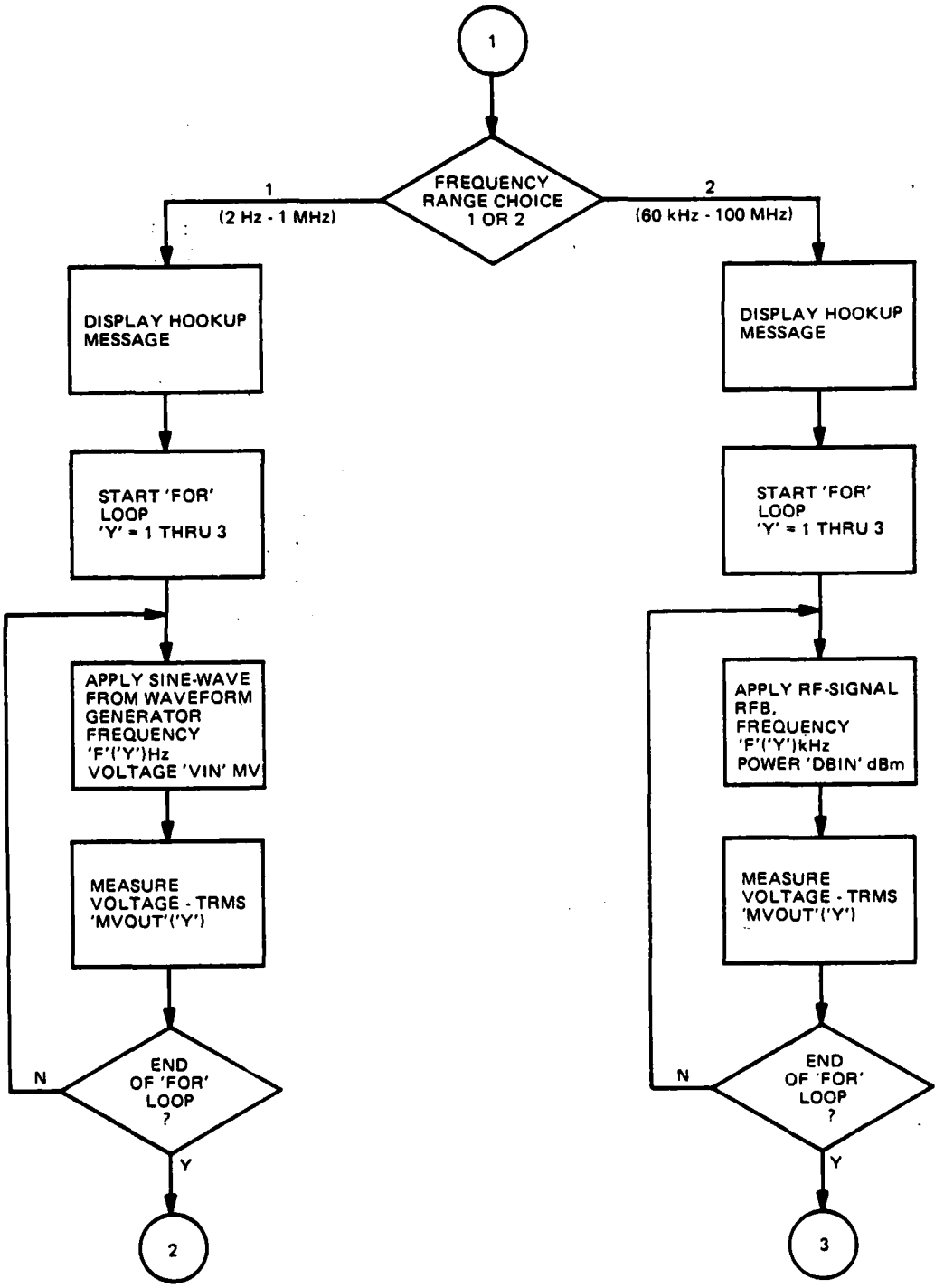
3.14 Filter Output Impedance Test Flow Chart

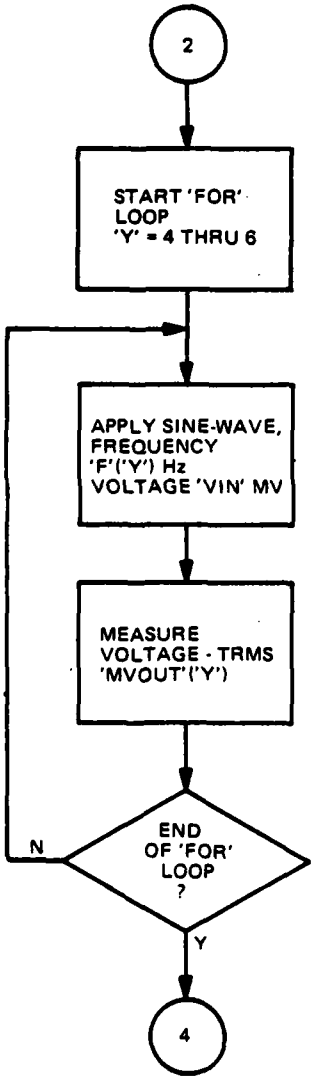


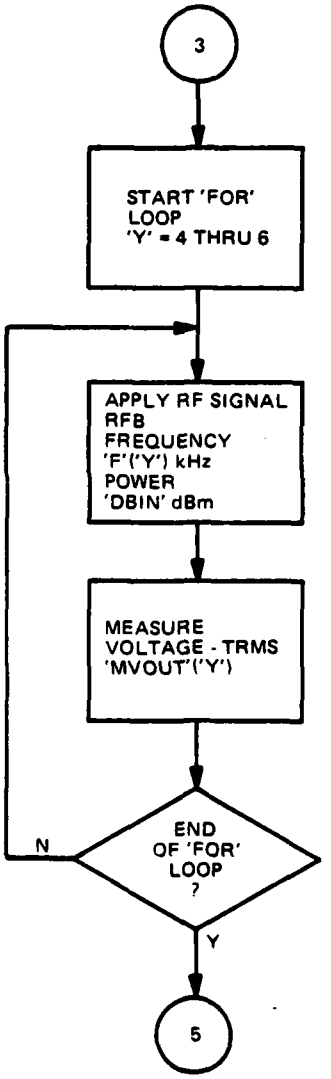

1
2
MEASURE VOLTAGE - TRMS WITH LOAD RL AND RT AT UUT O/P 'V2'
MEASURE DC VOLTS REFLECTED SIGNAL FROM UUT O/P 'VR'
CALCULATE OUTPUT IMPEDANCE FROM MEASURED VALUES 'ZOUT'
CALCULATE OUTPUT IMPEDANCE FROM MEASURED VALUES 'ZOUTH' 'ZOUTL'
RECORD INPUT IMPEDANCE FROM MEASURED VALUES 'ZOUT'
RECORD INPUT IMPEDANCE FROM MEASURED VALUES 'ZOUTH' 'ZOUTL'
RECORD UPPER AND LOWER LIMITS 'ZOUTUL' 'ZOUTLL'
FINISH

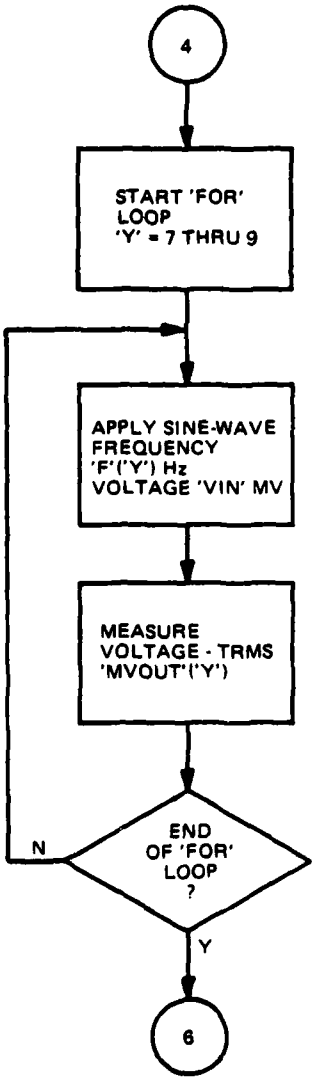
3.15 Filter Amplitude Response Test Flow Chart

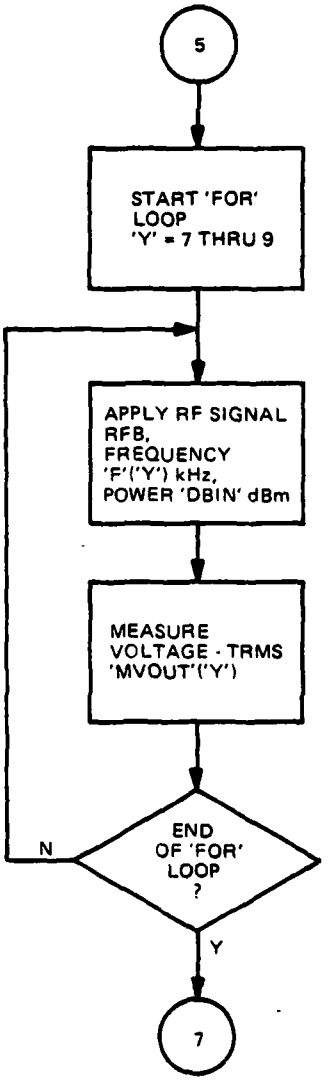


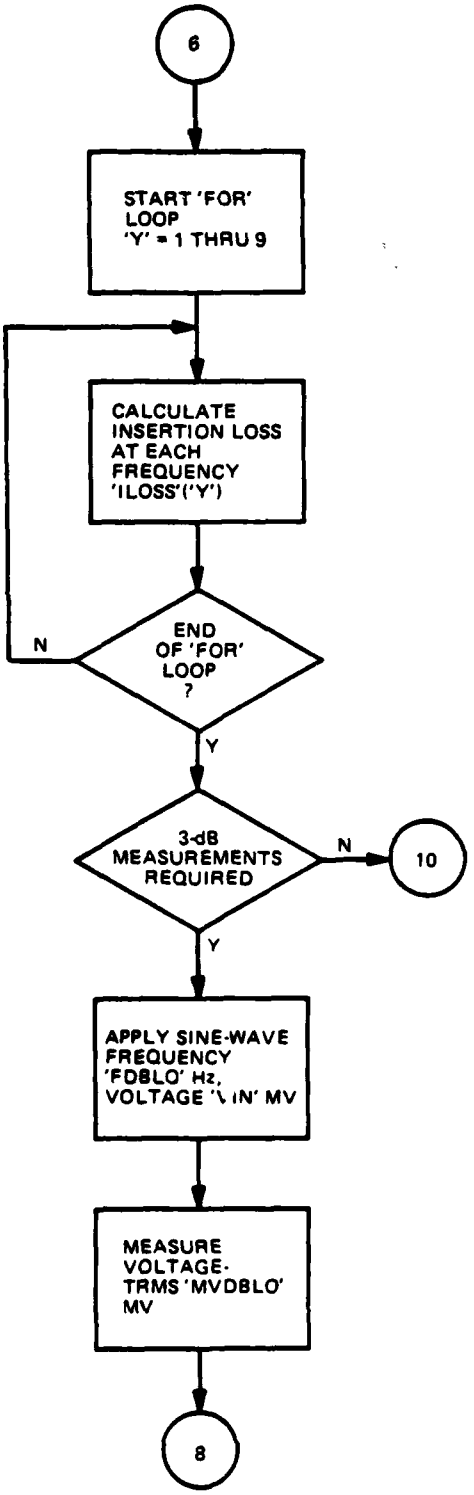

1
FREQUENCY RANGE CHOICE 1 OR 2
1
(2 Hz - 1 MHz)
2
(60 kHz - 100 MHz)
DISPLAY HOOKUP MESSAGE
START 'FOR' LOOP 'Y' = 1 THRU 3
APPLY SINE-WAVE FROM WAVEFORM GENERATOR FREQUENCY 'F'('Y')Hz VOLTAGE 'VIN' MV
MEASURE VOLTAGE - TRMS 'MVOUT'('Y')
END OF 'FOR' LOOP ?
N
Y
2
DISPLAY HOOKUP MESSAGE
START 'FOR' LOOP 'Y' = 1 THRU 3
APPLY RF-SIGNAL RFB, FREQUENCY 'F'('Y')kHz POWER 'DBIN' dBm
MEASURE VOLTAGE - TRMS 'MVOUT'('Y')
END OF 'FOR' LOOP ?
N
Y
3

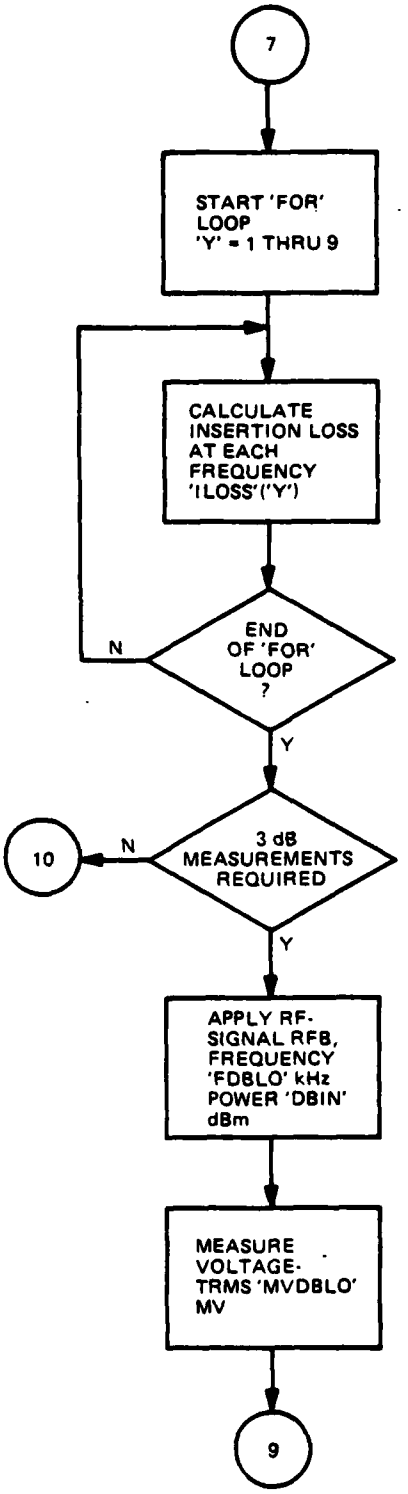

2
START 'FOR' LOOP 'Y' = 4 THRU 6
APPLY SINE-WAVE, FREQUENCY 'F'('Y') Hz VOLTAGE 'VIN' MV
MEASURE VOLTAGE - TRMS 'MVOUT'('Y')
END OF 'FOR' LOOP ?
N
Y
4

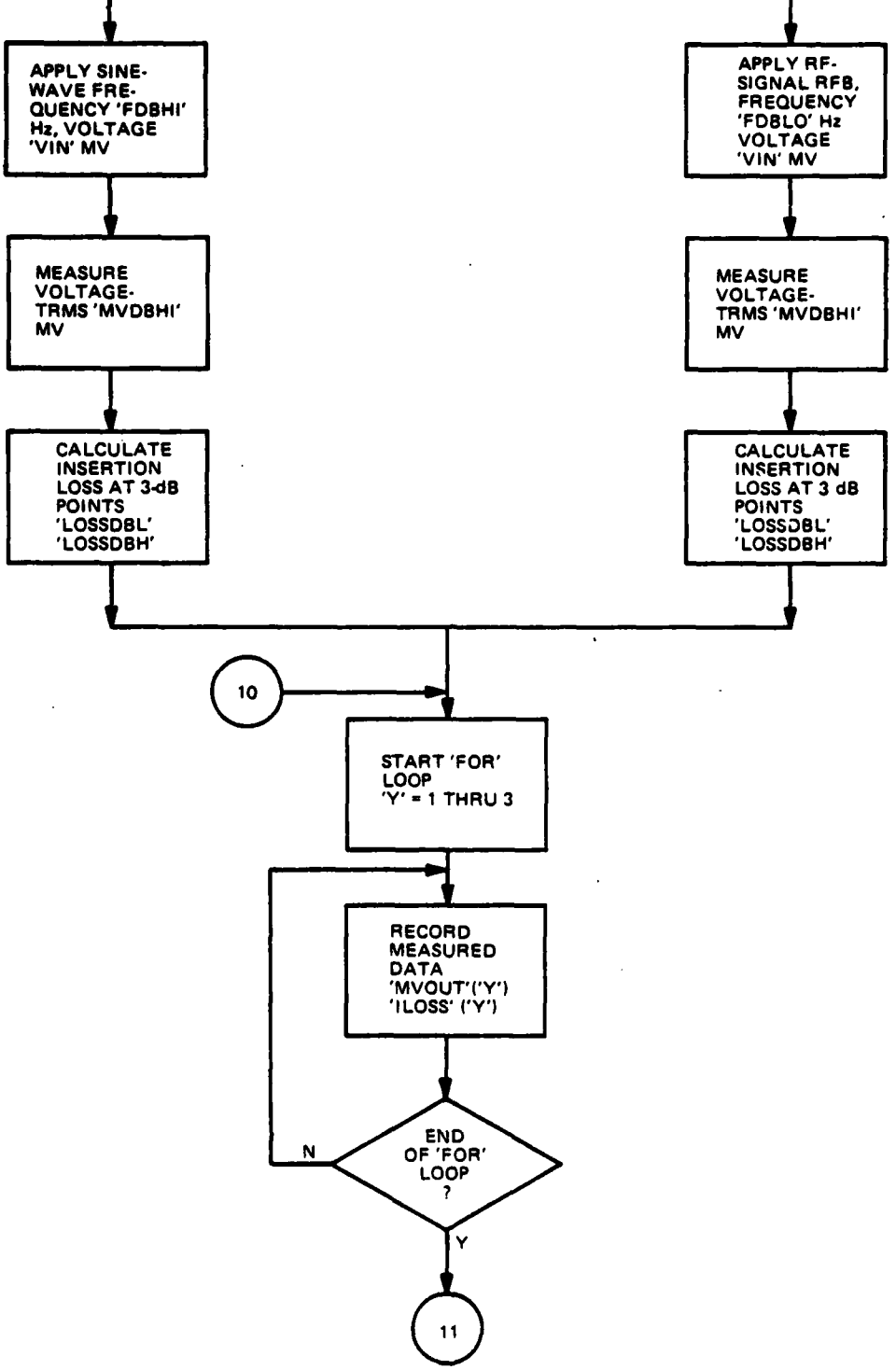

3
START 'FOR' LOOP 'Y' = 4 THRU 6
APPLY RF SIGNAL RFB FREQUENCY 'F'('Y') kHz POWER 'DBIN' dBm
MEASURE VOLTAGE - TRMS 'MVOUT'('Y')
END OF 'FOR' LOOP ?
N
Y
5

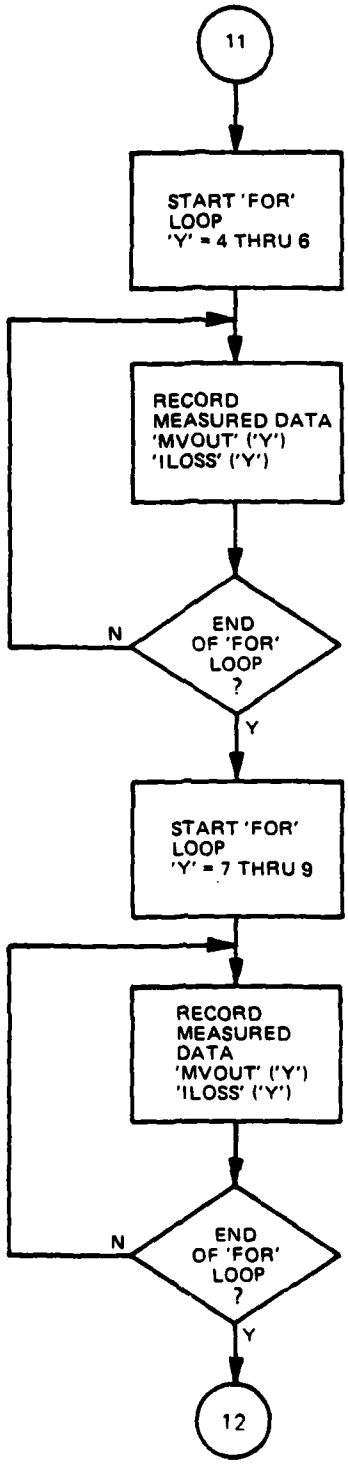

4
START 'FOR'
LOOP
'Y' = 7 THRU 9
APPLY SINE-WAVE
FREQUENCY
'F'('Y') Hz
VOLTAGE 'VIN' MV
MEASURE
VOLTAGE - TRMS
'MVOUT'('Y')
END
OF 'FOR'
LOOP
?
N
Y
6

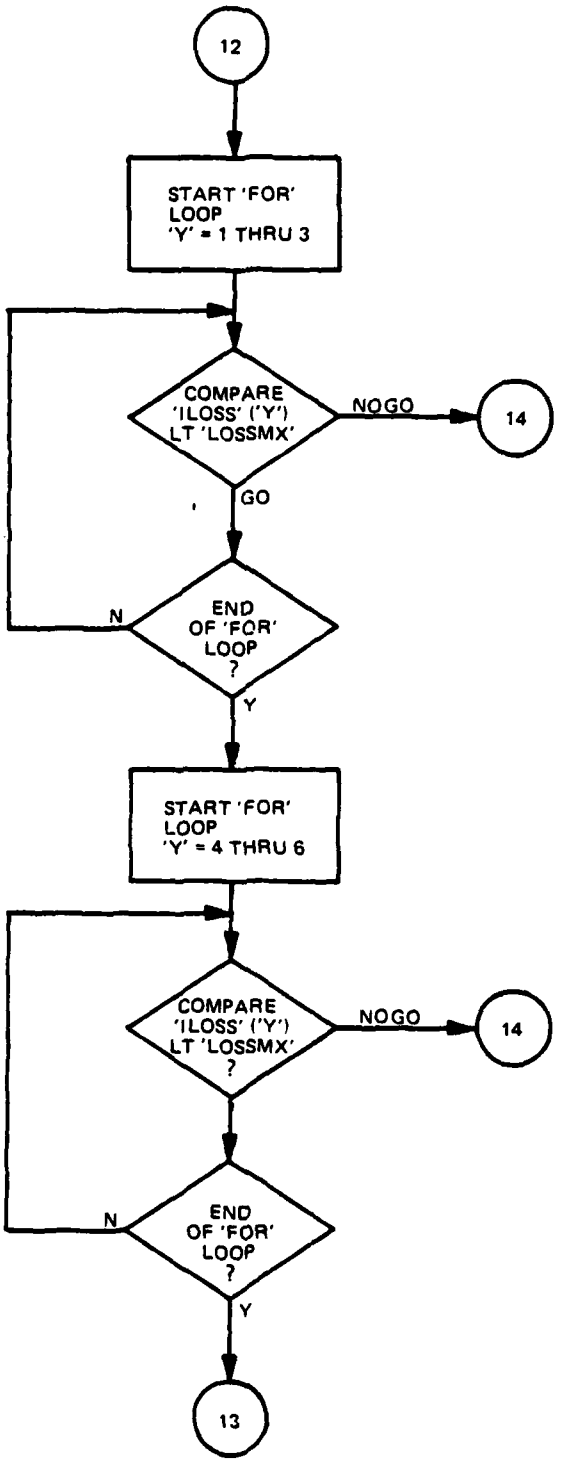

5
START 'FOR'
LOOP
'Y' = 7 THRU 9
APPLY RF SIGNAL
RFB,
FREQUENCY
'F'('Y') kHz,
POWER 'DBIN' dBm
MEASURE
VOLTAGE - TRMS
'MVOUT'('Y')
END
OF 'FOR'
LOOP
?
N
Y
7

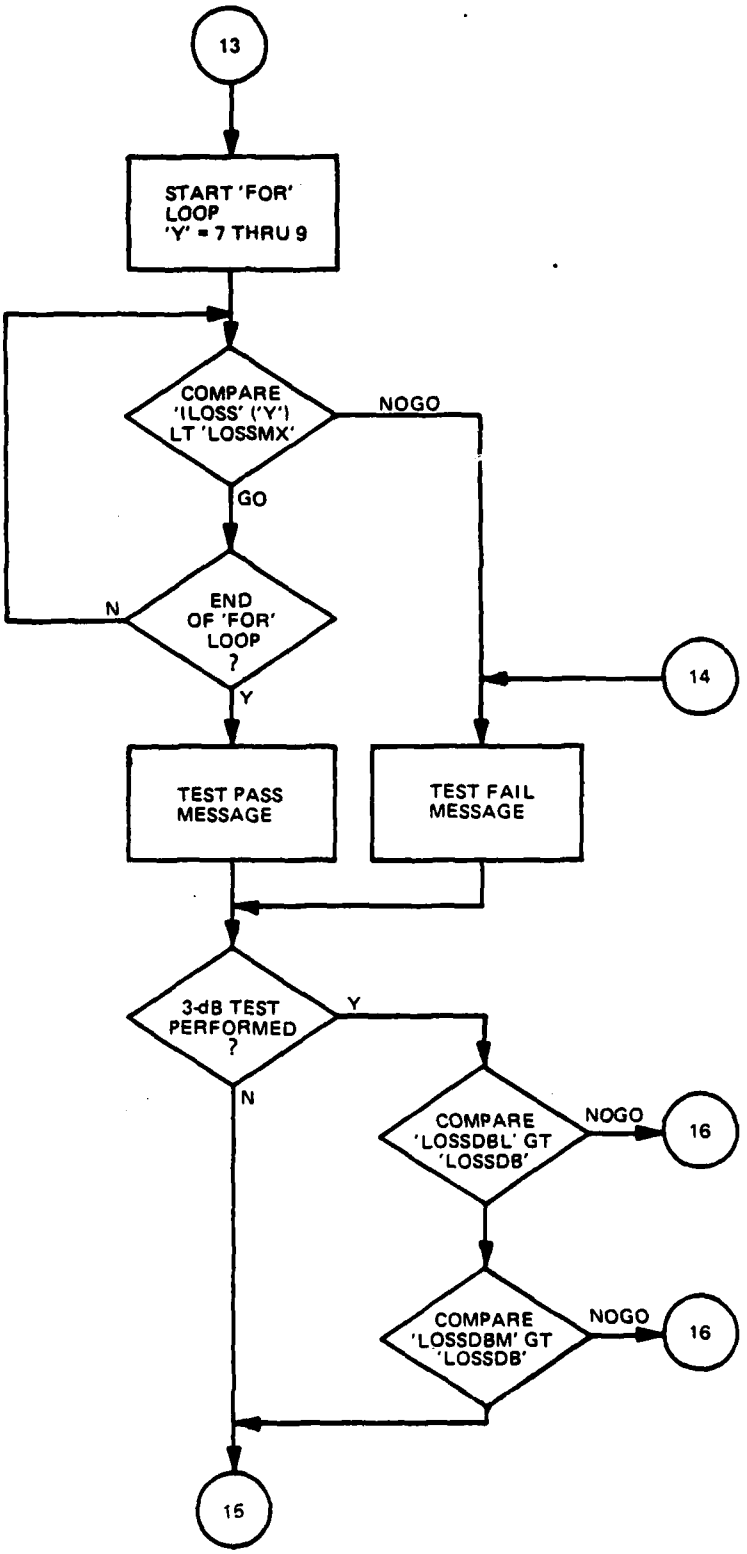

6
START 'FOR' LOOP 'Y' = 1 THRU 9
CALCULATE INSERTION LOSS AT EACH FREQUENCY 'ILOSS'('Y')
END OF 'FOR' LOOP ?
N
Y
3-dB MEASUREMENTS REQUIRED
N
10
Y
APPLY SINE-WAVE FREQUENCY 'FDBLO' Hz, VOLTAGE 'VIN' MV
MEASURE VOLTAGE-TRMS 'MVDBLO' MV
8

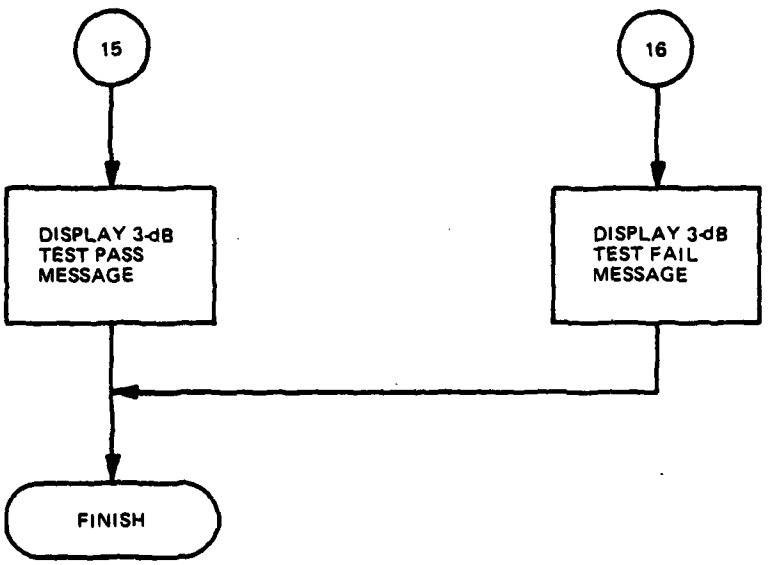

7
START 'FOR' LOOP 'Y' = 1 THRU 9
CALCULATE INSERTION LOSS AT EACH FREQUENCY 'ILOSS'('Y')
END OF 'FOR' LOOP ?
N
Y
10
N
3 dB MEASUREMENTS REQUIRED
Y
APPLY RF-SIGNAL RFB, FREQUENCY 'FDBLO' kHz POWER 'DBIN' dBm
MEASURE VOLTAGE-TRMS 'MVDBLO' MV
9


8
9
APPLY SINE-WAVE FREQUENCY 'FDBHI' Hz, VOLTAGE 'VIN' MV
APPLY RF-SIGNAL RFB, FREQUENCY 'FDBLO' Hz VOLTAGE 'VIN' MV
MEASURE VOLTAGE-TRMS 'MVDBHI' MV
MEASURE VOLTAGE-TRMS 'MVDBHI' MV
CALCULATE INSERTION LOSS AT 3-dB POINTS 'LOSSDBL' 'LOSSDBH'
CALCULATE INSERTION LOSS AT 3 dB POINTS 'LOSSDBL' 'LOSSDBH'
10
START 'FOR' LOOP 'Y' = 1 THRU 3
RECORD MEASURED DATA 'MVOUT'('Y') 'ILOSS' ('Y')
END OF 'FOR' LOOP ?
N
Y
11


11
START 'FOR' LOOP 'Y' = 4 THRU 6
RECORD MEASURED DATA 'MVOUT' ('Y') 'ILOSS' ('Y')
END OF 'FOR' LOOP ?
N
Y
START 'FOR' LOOP 'Y' = 7 THRU 9
RECORD MEASURED DATA 'MVOUT' ('Y') 'ILOSS' ('Y')
END OF 'FOR' LOOP ?
N
Y
12

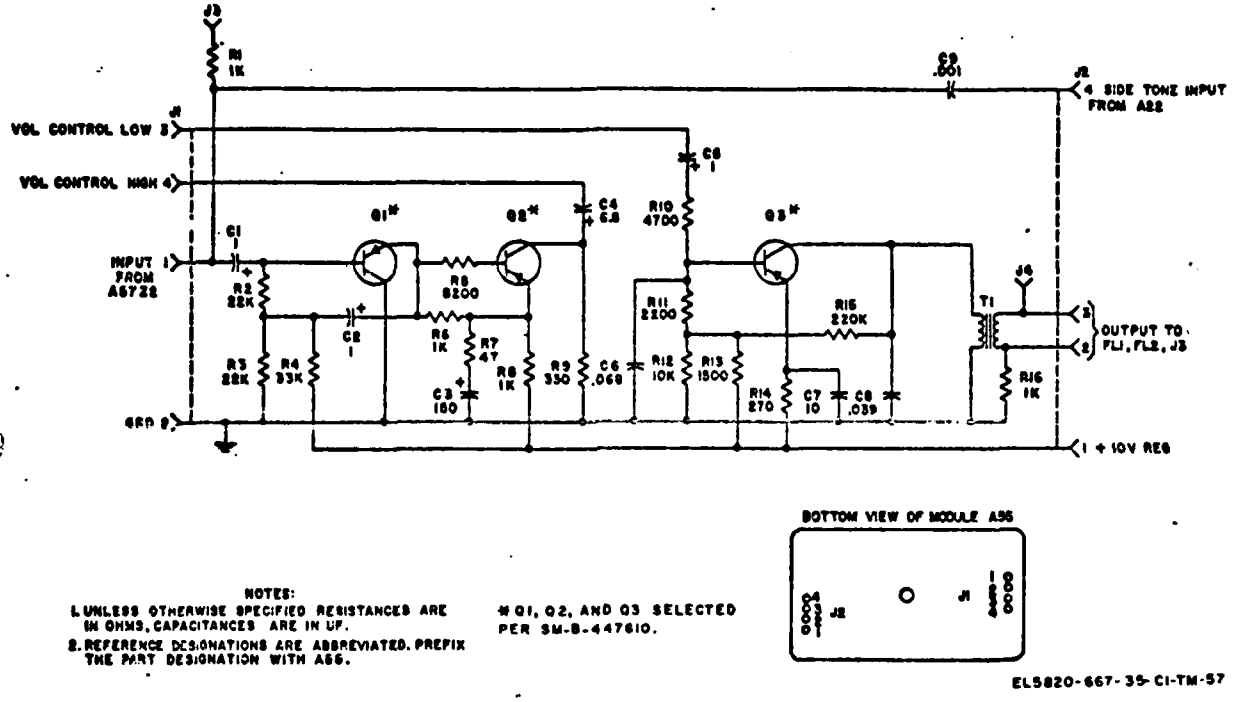

12
START 'FOR' LOOP 'Y' = 1 THRU 3
COMPARE 'ILOSS' ('Y') LT 'LOSSMX'
NOGO
14
GO
END OF 'FOR' LOOP ?
N
Y
START 'FOR' LOOP 'Y' = 4 THRU 6
COMPARE 'ILOSS' ('Y') LT 'LOSSMX' ?
NOGO
14
END OF 'FOR' LOOP ?
N
Y
13


13
START 'FOR' LOOP 'Y' = 7 THRU 9
COMPARE 'ILOSS' ('Y') LT 'LOSSMX'
NOGO
GO
END OF 'FOR' LOOP ?
N
Y
14
TEST PASS MESSAGE
TEST FAIL MESSAGE
3-dB TEST PERFORMED ?
Y
N
COMPARE 'LOSSDBL' GT 'LOSSDB'
NOGO
16
COMPARE 'LOSSDBM' GT 'LOSSDB'
NOGO
16
15


15
16
DISPLAY 3-dB TEST PASS MESSAGE
DISPLAY 3-dB TEST FAIL MESSAGE
FINISH

SECTION IV

Schematics of AGEN II Units Under Test



NOTES:

1. UNLESS OTHERWISE SPECIFIED RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UF.
2. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE PART DESIGNATION WITH A55.

* Q1, Q2, AND Q3 SELECTED PER SM-B-447610.

EL5820-667-35-CI-TM-57

Fig. 4-1 *Receiver audio amplifier module A55, schematic diagram.*

4.1 Receiver Audio Amplifier Module A55

Receiver audio amplifier module A55 amplifies the audio output from the 11.5-mc discriminator Z2, or amplifies the sidetone from module A22 and applies it to the handset.

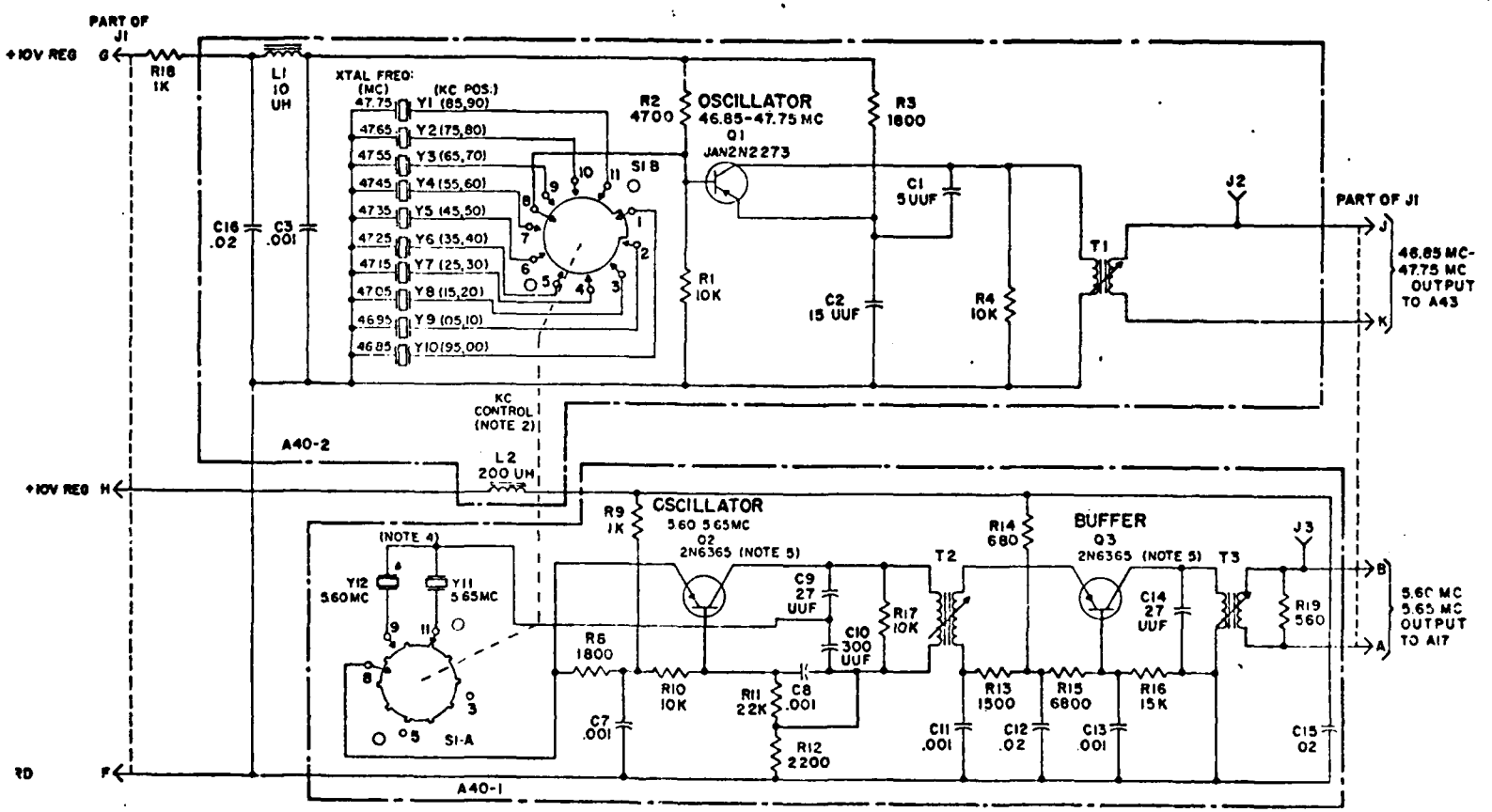
a. The audio output from Z2 is coupled through coupling capacitor C1 to the base of emitter follower Q1. The output of Q1 is developed across resistors R6 and R7 and is resistively coupled to the base of Q2 through R5. The output of Q2, developed across resistor R9, is coupled by capacitor C4 to VOLUME control R1 (on the front panel), to pin P of POWER plug J3 (on the front panel) for wideband audio output and to tone squelch module A54 . Capacitor C2 provides negative feedback to the base of Q1 through resistor R2. Capacitor C3 acts as a bypass to reduce Q2 emitter degeneration to resistor R7. Resistor R6 also provides the degenerative feedback from Q2 emitter. This degenerative feedback minimizes audio distortion, and provides a high input impedance to prevent the loading of Z2. The base-to-emitter bias for Q1 is provided by resistors R3 and R4; resistors R5, R6, and R8 establish the operating bias for Q2.

b. Since the first two audio stages have very wide bandwidth, the audio signal at the moving contact of the VOLUME control is applied through coupling capacitor C5 to the low-pass filter comprised of resistor R10 and capacitor C6. Resistor R10 and capacitor C6 attenuate the higher audiofrequencies, and pass voice signals to the base of amplifier Q3. The base bias for transistor Q3 is provided by resistors R12 and R13. The emitter swamping resistor, R14, is bypassed by capacitor C7. The output signal at the collector of Q3 drives the primary of audio transformer T1. Resistors R11 and R15 provide a degenerative feedback which reduces the output impedance of Q3 to match the primary impedance of T1. Capacitor C8 shapes the high frequency response at the collector of Q3. The resulting audio output is fed to the handset through filter network FL1 or FL2 and pin B of POWER plug J3 (on the front panel).

c. The input to audio amplifier module A55 can be measured through isolation resistor R1 at test jack J3. The output of A55 can be measured at test jack J4.

d. During transmission, the sidetone audio is coupled from module A22 through capacitor C9 to the input circuit of Q1. In the SQUELCH and RETRANS modes, resistor R16 properly terminates this audio module (A55) while relay K3 is not activated since the output at J4 is grounded.

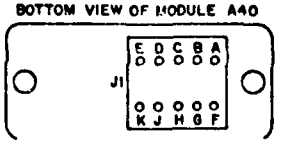
e. Capacitor C11 (in the chassis) is an RF bypass capacitor on the +10-volt regulated input to module A55.



NOTES:

1. UNLESS OTHERWISE SPECIFIED, RESISTANCE ARE IN OHMS, CAPACITANCE ARE IN UF.
2. SWITCH SHOWN IN 30.00 MC POSITION OF THE KC TUNING CONTROL ON THE FRONT PANEL.
3. REFERENCE DESIGNATIONS ARE ABBREVIATED, PREFIX THE PART DESIGNATION WITH A40.

BOTTOM VIEW OF MODULE A40



4. 5.65 MC ± 500 CPS ON EVEN POSITIONS OF KC CONTROL (00, 10, 20, 30, ETC); 5.60 MC ON ODD POSITIONS (05, 15, 25, 35 ETC)
5. Q2 AND Q3 ARE TYPE 2N2273 IN SOME UNITS.

EL5820-667-35-CI-TM-60

Fig. 4-2 *Interval oscillator module A40, schematic diagram.*

4.2 Interval Oscillator Module A40

Interval oscillator module A40 supplies the Iss with two crystal-controlled signals. This module has two crystal-controlled oscillators: Q1 generates frequencies of 46.85 mc to 47.75 mc in 100-kc increments, and Q2 generates frequencies of 5.60 and 5.65 mc. The 10-volt B+ is applied to the module during the transmit and receive modes. The frequencies of the two oscillators are the same for both modes.

a. Oscillator Q1, 46.85 to 47.75 Mc.

(1) Transistor Q1 is connected in a crystal-controlled oscillator that uses 1 of 10 crystals. Crystal selection is determined by the kc tuning control on the front panel through switch S1B. The tuned collector circuit is composed of capacitors C1 and C2 and the primary of transformer T1. Oscillation is sustained by feeding back part of the energy in the collector bank through capacitor C1 to the emitter. Resistor R4 is the tuned circuit damping resistor. The crystal supplies low impedance to base Q1 at the frequency of series resonance to provide sufficient gain for oscillation.

(2) Resistors R1 and R2 form a voltage-divider network which develops the base bias for Q1. Resistor R3 is the emitter swamping resistor. Resistor R18, inductor L1, and capacitors C16 and C3 form a filter network in the +10-volt supply to Q1. The rf output of Q1 can be measured at test J2.

(3) As switch S1B is rotated by the kc tuning control from 0.00 to 0.95 mc the sequence of frequencies will be: once 46.85: twice each 46.95, 47.05, 47.15, 47.25, 47.35, 47.45, 47.55, 47.65, 47.75; and finally 46.85 again.

b. Oscillator Q2, 5.60 or 5.65 Mc.

(1) Transistor Q2 is connected in a crystal-controlled oscillator circuit that uses one of two crystals to generate the frequency reference for phase comparison in module A17. The tuned collector circuit is made up of capacitors C9 and C10 and the primary of transformer T2. Oscillation is sustained by feeding back part of the energy in the collector circuit from the junction of C9 and C10 to the selected crystal ((2) below), and the contacts of S1A to the emitter of Q2; this action completes the regenerative circuit.

(2) Crystal selection is determined by the frequency selected by the kc tuning control on the front panel. If the RT-841/PRC-77 is operating on a 100-kc channel (31.10 mc, 74.20 mc, etc), S1A will be in the position shown on figure 7-24 and crystal Y11 (5.65 mc) will be selected through contacts 8 and 11 of S1A; this action completes the regenerative circuit to the emitter of Q2. If the RT-841/PRC-77 is operating on a 50-kc channel (31.15 mc, 74.25 mc, etc), S1A will be turned clockwise one position from that shown and crystal Y12 (5.60 mc) will be connected through contacts 8 and 9 of S1A; this action completes the regenerative circuit to the emitter of Q2.

(3) Capacitor C7 is an RF bypass capacitor. Capacitor C8 is a coupling capacitor between the base and collector circuit. Resistors R10, R11, and R12 develop fixed bias; resistors R8 and R9 are emitter swamping resistors for Q2.

c. Buffer Q3.

(1) The output from oscillator Q2 is coupled through transformer T2 to the base and emitter of Q3. The buffer isolates Q2 from any varying loading effects.

(2) Resistors R14, R15, and R16 develop fixed-base bias. Resistor R13 is the emitter swamping resistor. Capacitors C11, C12, and C13 are RF bypass capacitors. Inductor L2 and capacitor C15 form a decoupling network to prevent RF leakage into the power supply. The RF output from Q3 can be measured at test jack J3.

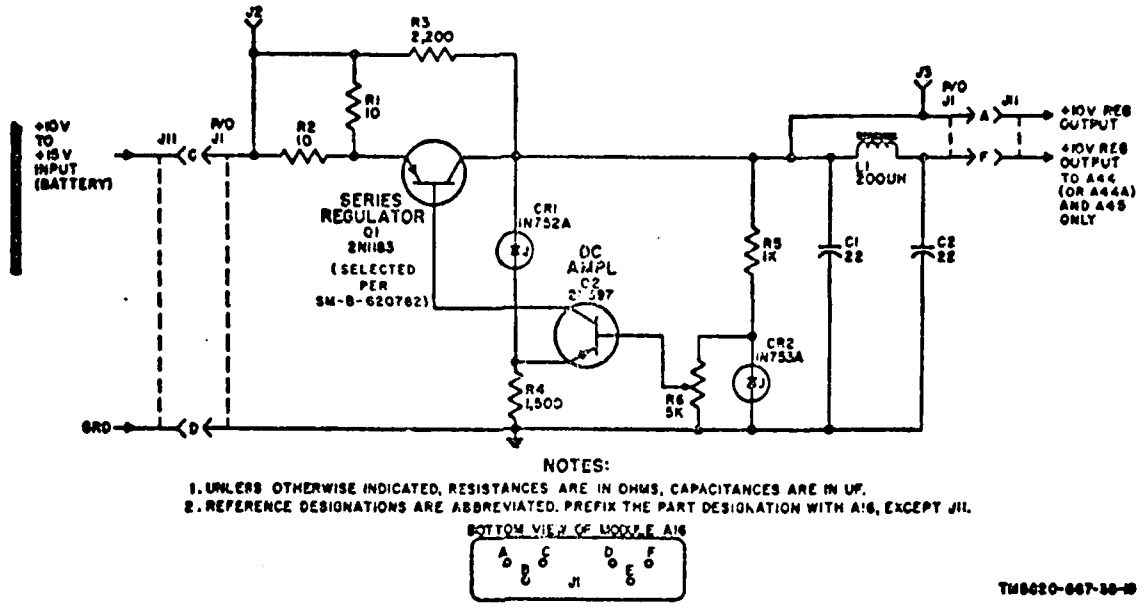


Fig. 4-3 *Voltage regulator module A16, schematic diagram.*

4.3 Voltage Regulator Module A16

The voltage regulator circuit supplies the entire fss, including the vfo, with a regulated +10 volts dc (+9.5 volts dc nominal). The regulator uses a high power germanium transistor (Q1) as a series regulator in conjunction with a medium-power silicon transistor (Q2). Transistor Q2 operates as a dc amplifier. The combination of resistor R5, potentiometer R6, and diode CR2 form a constant reference voltage source for the base of the dc amplifier. The combination of diode CR1 and emitter resistor R4 forms a voltage divider. Any variation in output voltage appears across resistor R4, since CR1 maintains a constant voltage drop. When the output voltage increases due to a decrease in load or an increase in the input voltage, a proportional positive voltage increase appears at the emitter of dc amplifier Q2 and results in less current flow through Q2. The base of series regulator Q1 goes more positive; conduction through Q1 decreases, which effectively increases the impedance of series regulator Q1. The effect is a decrease in the regulator output; the circuit has compensated for the increase in output voltage. The opposite series of events takes place when the output voltage decreases because of a load increase or input voltage decrease. Potentiometer R6 varies the output voltage of the voltage regulator to provide a nominal output of 9.5 volts dc. The regulator provides two +10-volt outputs, one filtered and one unfiltered. The filtered output is filtered by a pi-filter network consisting of coil L1 and capacitors C1 and C2. The filtered output is supplied to modules A44 and A45 . The unfiltered output is supplied to the remainder of the circuits requiring regulated +10 volts. The unregulated input voltage to module A16 can be measured at test jack J2; the regulated output voltage from module A16 can be measured at test jack J3.

Note. All references to +10 volts dc regulated imply that voltage regulator A16 supplies this voltage. The nominal output of A13 is +9.5 volts dc.

4.4 Frequency Synthesizer System Second Mixer Module A12

The fss second mixer module heterodynes the output from 53-mc filter A43 with the 46.85- to 47.75-mc output of the 100-kc interval oscillator (applied through A43) to produce an fss IF of 5.60 or 5.65 mc. This output is applied to fss IF amplifier module A18.

a. The 53-mc input from module A43 is coupled through capacitor C1 to the base of Q1. The 46.85- to 47.75-mc input from A43 is coupled through capacitor C2 to the emitter of Q1. Transistor Q1 heterodynes these two input signals; the resultant output signals at the collector of Q1 are applied to the frequency selective network.

b. The frequency selective network is composed of capacitors C4 through C7, variable transformers T1 and T2, and variable inductors L1 and L2. The outputs from Q1 are the two original frequencies plus their sum and difference. The frequency selective network passes only the difference frequency. The network is a bandpass filter which has a flat characteristic resonant frequency of 5.6 mc.

c. Resistor R5 and capacitor C8 filter RF signals from the +10-volt dc supply. Resistors R1 and R2 provide the fixed-base bias. Resistor R3 is the emitter swamping resistor. Resistors R4 and R6 terminate the filter properly and minimize variations due to the varying impedances of transistors. The radiofrequency (RF) output of module A12 can be measured at test jack J2.

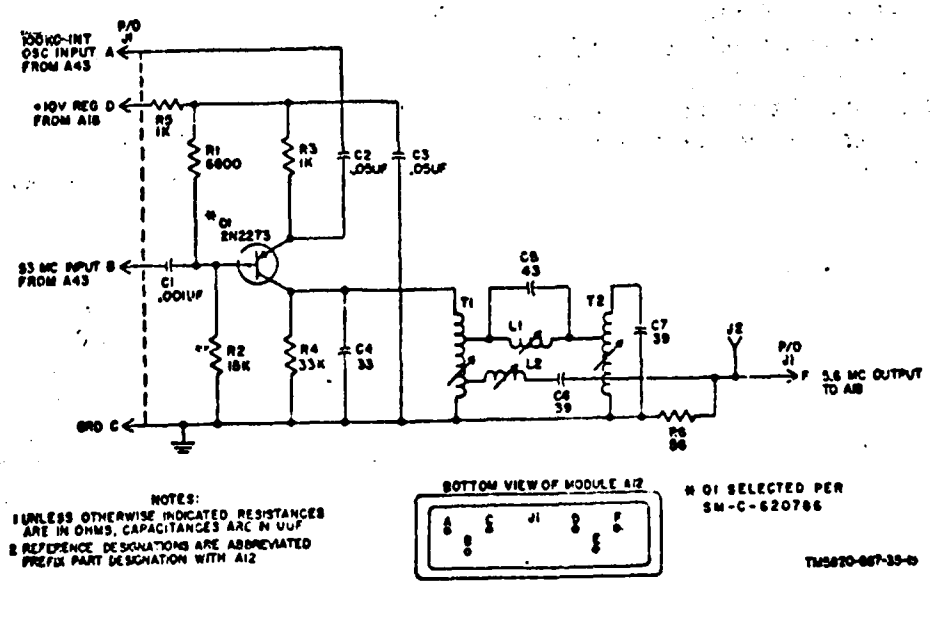


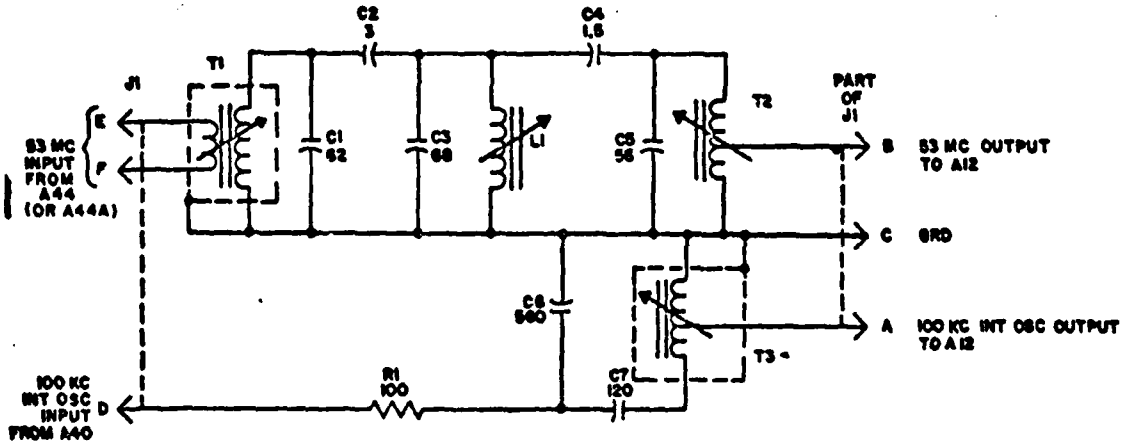
Fig. 4.4 *Frequency synthesizer system second mixer module A12, schematic diagram.*

4.5 Filter A43, 53-Mc

The 53-mc filter has two input signals.

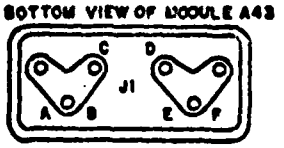
a. The output signal from 100-kc interval oscillator module A40 is coupled through isolation resistor R1 and a matching network consisting of capacitors C6 and C7 and transformer T3 to fss second mixer module A12 (para 2-26). This circuit minimizes spurious frequency injection into the second mixer.

b. The 53-mc signal from first mixer module A44 is coupled to the filter through transformer T1 to a triple-tuned network. The three tuned circuits are the secondary of T1 and C1, L1 and C3, T2 and C5. Capacitors C2 and C4 are coupling capacitors. This triple-tuned network provides a 2-mc bandpass at the 3-decibel (db) points. The output of this network is coupled to second mixer module A12.



NOTES:

1. UNLESS OTHERWISE INDICATED, RESISTANCES ARE IN OHMS, CAPACITANCES ARE IN UUF.
2. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE PART DESIGNATION WITH A43.



TM5820-667-35-14

Fig. 4.5 *53-megacycle filter module A43, schematic diagram.*

SECTION V

Schematic and Diagram of AGEN II Interface Device

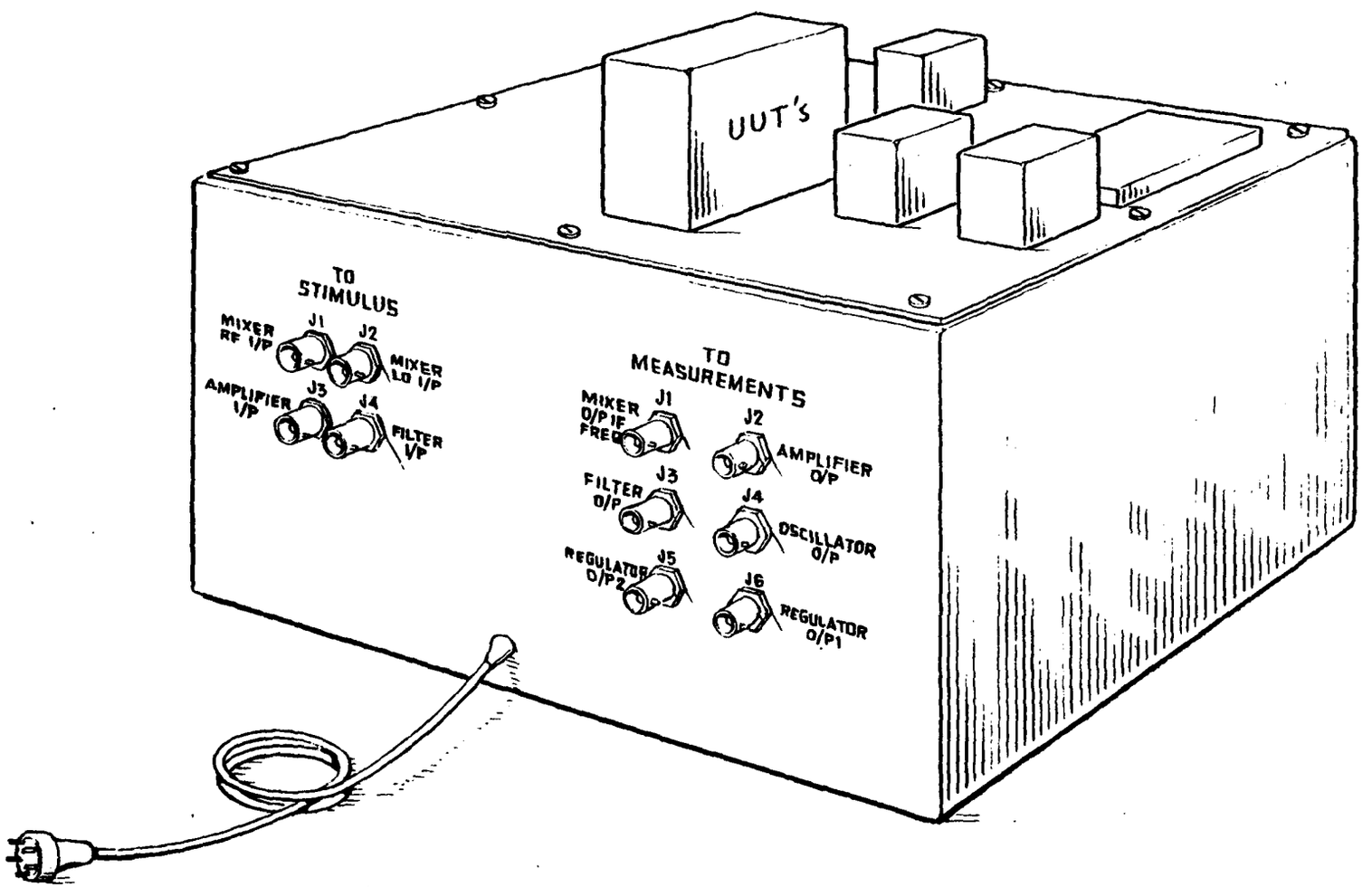
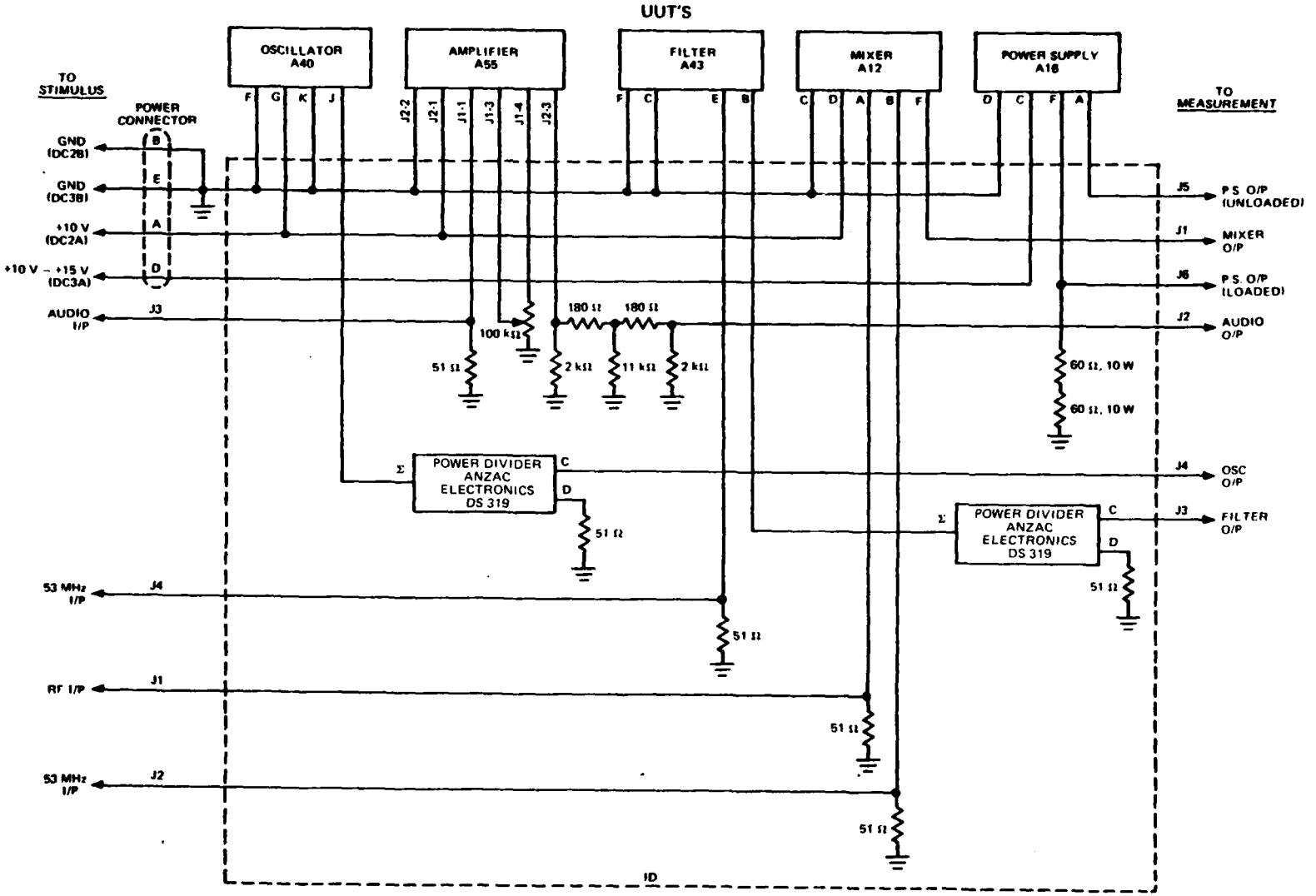


Figure 5-1. Diagram of AGEN II Interface Device (ID)



NOTE:

(1) ALL UNUSED PINS OF DS 319 ARE CONNECTED TO GROUND.
(2) POWER CONNECTOR IS P/N MS3126F-14-SP.
(3) ALL CONNECTORS ARE BNC, FEMALE.
(4) ALL RESISTORS ARE 1/4W, UNLESS OTHERWISE SPECIFIED.

Figure 5-2. Schematic of AGEN II ID

SECTION VI

MODEM SYSTEM

6.1 MODEM Description

Since the EQUATE test station and the AGEN source code generator are not situated at the same location, a MODEM system has been designed to link the two locations together through a telephone line. This MODEM system consists of the following items:

a) Omnitec Acoustic Coupler , Model 710, 300 BAUD, Full Duplex

b) Data General MODEM Controller, Part No. 4029, I/O Controller with 300 BAUD.

c) MODEM Cable

d) MODEM Protocal Software Program Tape.

Figure 6-1 shows the wiring diagram of the MODEM Cable and its connection to the EQUATE Program Development Center (PDC). Table 6-1 contains the source listing of the MODEM protocal software program.

In order to connect the MODEM system to the PDC, remove power of the PDC and replace the I/O Controller in the computer by the MODEM Controller (I/O Controller with 300 BAUD). Connect the MODEM Cable as shown in Figure 6-1 and set the foreground terminal to 300 BAUD and half-duplex. Turn the power back on the PDC and load the MODEM Protocal Program tape on the PDC. Transfer data from the MODEM Protocal Program tape to the PDC disc by typing the following:

```
INIT   MTØ
LOAD/V MTØ : Ø
```

The names of files such as COMMO.SV, CHAR.LS, COMMO.FR, CHAR.RB, and CHAR.SR will appear on the CRT. The MODEM Protocal Program is now resident in the PDC and ready to control any MODEM connection between the PDC and the AGEN II source code generator resident at PRD, Syosset, New York.

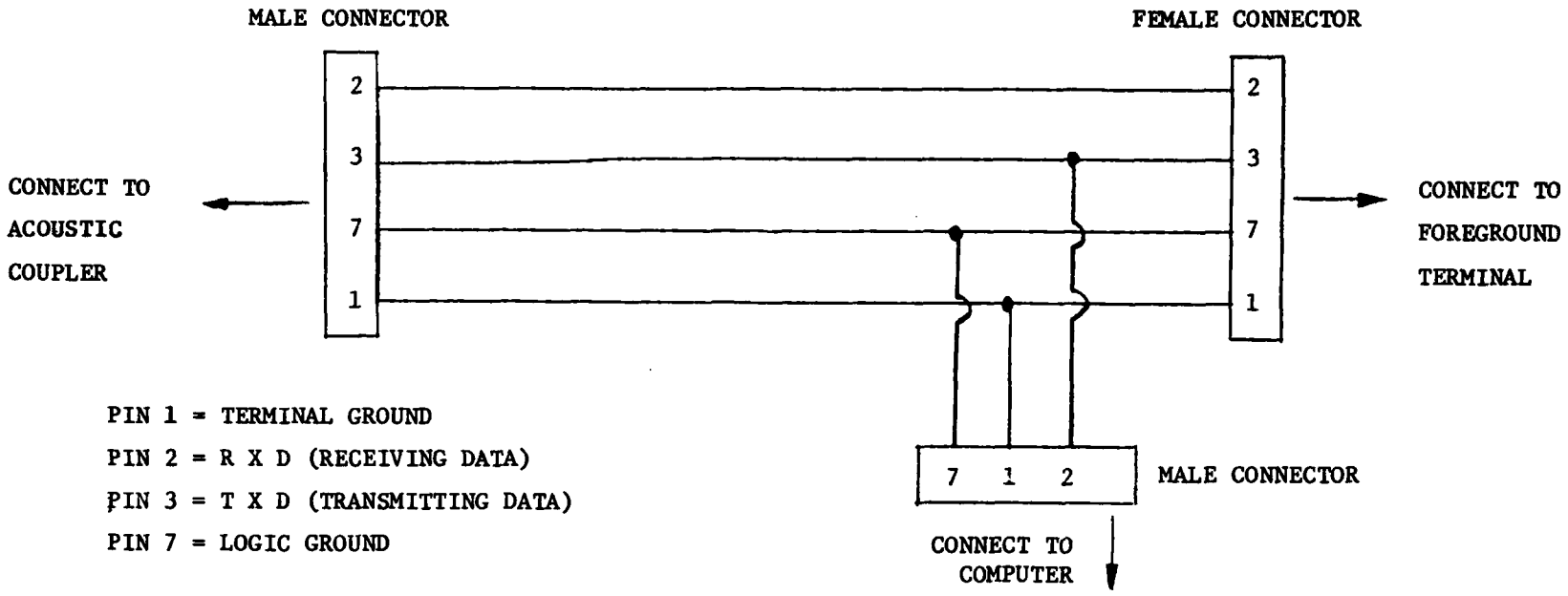


FIGURE 6-1 MODEM CABLE

```
C
C
C
      THIS PROGRAM WILL INTERRACT WITH THE OPERATOR IN SUCH A MANNER
C     AS TO BLIND THE DATA GENERAL MACHINE TO THE EXISTENCE OF ANOTHER
C     COMPUTER  UNIVAC 1108
C
C
C     EDITED 2/21/80 REV 1
C
      DIMENSION MCAR0(80),MCAR1(80),MCAR2(4)
      COMMON /LBL/NPROM1(1),NPROM2(1),NPROM3(4),NPROM4(6),NPROM5(1),NPROM6(5)
      DATA NPROM1/'> '/,NPROM2/'R '/,NPROM5/'K '/
      DATA NPROM3/'  ','B ','O ','T '/
      DATA NPROM4/'  ','C ','  ','E ','O ','T '/
C
C     THE FIRST FILE WILL BE TAPE00
C     INITIALIZE SOME CONSTANTS
C
      NUM=0
      NUM1=124K          ;WE GOT A START TAPE ORDER
      NUM2=40K           ;SPACE CHARACTER
      NUM3=76K           ;1108 PROMPT
      NUM4=103K          ;C - DENOTING A COMMENT
      NUM5=113K          ;K - DENOTING A TAPE NUMBER
      NUM6=0             ;ITERATION COUNTER
C
C
      SIGN-ON FOR 1108
C
C
C
900   MCAR2(1)="TA"
      MCAR2(2)="PE"
      MCAR2(4)=0
      NUB1=NUM/10
      NUB2=NUM-NUB1*10
      NUB3=30060K+(256*NUB1+NUB2)
      MCAR2(3)=NUB3
C
C
C     FIRST WE DELETE THE FILE IF IT EXISTS
C
      CALL DFILE(MCAR2,IER)
C
C     NOW OPEN A NEW FILE WITH THAT NAME
C
      CALL OPEN(2,MCAR2,3,IER)
      IF(IER.NE.1) GOTO 550
925   CALL CHAR(INEW)
      CALL FOPEN(1,'$TTI1')
      CALL FOPEN(0,'$TTO1')
215   READ(1,220) MCAR1
220   FORMAT(80A1)
      WRITE(2,250) MCAR1
250   FORMAT(1X,80A1)
      IF(NCOMP(MCAR1,1,6,NPROM4,1))215,500,215
```

TABLE 6-1 MODEM PROTOCAL PROGRAM (SHEET 1 OF 4)

```
C
C       CLOSE THE FILE
C
300     CALL CLOSE(2,IER)
        IF(IER.NE.1) GOTO 300
        NUM=NUM+1



        CALL CLOSE(0,IER)
        IF(IER.NE.1) GOTO 550
        CALL CLOSE(1,IER)
        IF(IER.NE.1) GOTO 550
        GOTO 900
C
C       EXIT   PROCESS
C
C       FIRST WE GET CLOSING ARGUMENTS FROM THE UNIVAC
C       NEXT WE SAY GOODBY(@FIN,@@TERM) TO UNIVAC
C       LAST WE TELL OPERATOR WHICH FILES HE CREATED
C       CLOSE ALL OPEN FILES, HANG UP THE PHONE AND GO BACK TO C L I
C
550     WRITE(10)" SIGN OFF UNIVAC 1108"
C
C       MAKE SURE ALL FILES ARE CLOSED
C
        CALL RESET
C
C       DATA TO OPERATOR
C
        WRITE(10,675) NUM
675     FORMAT(1X," YOU HAVE USED",I2," FILES")
        STOP
        END
```

TABLE 6-1 MODEM PROTOCAL PROGRAM (SHEET 2 OF 4)

```
        .TITL   CHAR
        .ENT    CHAR
        .EXTD   .CPYL,.FRET
        AR=     -167
        .FS=    1
        .NREL
        .FS
CHAR:   JSR     @.CPYL
        LDA     2,AR,3
MORE1:  SUBO    1,1
        STA     1,NUM
MORE:   SKPBZ   TTI1
        JMP     .-1
        DIAS    0,TTI1
        SKPBZ   TTO
        JMP     .-1
        DOAS    0,TTO
        LDA     1,PARITY
        AND     1,0
;       LDA     1,PROMPT
;       SUB#    1,0,SZR
        JMP     NEXT
BYE:    STA     0,0,2
        JSR     @.FRET
NEXT:   LDA     3,NUM
        MOV     3,3,SZR         ;NUM=0
        JMP     NEX2            ;NOT A ZERO
        LDA     1,PROM2         ;CHECK FOR A C
        SUB#    1,0,SZR
        JMP     MORE1           ;NOT A "C"
        ISZ     NUM             ;NUM=NUM+1
        JMP     MORE
NEX2:   LDA     1,ONE           ;NUM=1?
        SUB#    1,3,SZR         ;
        JMP     NEX3            ;NOT 1, CHECKK FOR 2
        LDA     1,PROM3         ;IS IT A SPACE
        SUB#    1,0,SZR
        JMP     MORE1           ;NOT A SPACE
        ISZ     NUM             ;NUM=NUM+1
        JMP     MORE
NEX3:   LDA     1,TWO           ;NUM=2?
        SUB#    1,3,SZR         ;
        JMP     NEX4            ;NOT A 2, MAYBE 3
        LDA     1,PROM4
        SUB#    1,0,SZR         ;SEE IF A "B"
        JMP     MORE1           ;NOPE
        ISZ     NUM             ;NUM=NUM+1
        JMP     MORE
```

TABLE 6-1 MODEM PROTOCAL PROGRAM (SHEET 3 OF 4)

```
NEX4:   LDA     1,THREE
        SUB#    1,3,SZR
        JMP     NEX5                    ;NOT A 3,SHOULD BE 4
        LDA     1,PROM5
        SUB#    1,0,SZR
        JMP     MORE1                   ;NOT AN "0"
        ISZ     NUM
        JMP     MORE
NEX5:   LDA     1,PROM6
        SUB#    1,0,SZR
        JMP     MORE1                   ;NOT A "T"
        JMP     BYE                     ;IT'S A C BUT, START SAVING
TTI1:   51
PARITY: 177
FOUR:   4


THREE:  3
TWO:    2
ONE:    1
PROM2:  103
PROM3:  40
PROM4:  102
PROM5:  117
PROM6:  124
NUM:    0
PROMPT: 76
TTO:    10
        .END
```

TABLE 6-1 MODEM PROTOCAL PROGRAM (SHEET 4 OF 4)

SECTION VII

TEST DATA OF AGEN II PROJECT VALIDATION

MAY 1, 1980

UUT: AMPAR.IC REV: 4/28/80 DATE: 5/1/80 9:19:11

MEASURED OUTPUT VOLTAGE1= 662MV
MEASURED OUTPUT VOLTAGE2= 723MV
MEASURED OUTPUT VOLTAGE3= 725MV
MEASURED OUTPUT VOLTAGE4= 692MV
MEASURED OUTPUT VOLTAGE5= 626MV

UUT PASSED AMPLITUDE RESPONSE TEST
TEST1. MEASURED GAIN= 28.54DB
TEST2. MEASURED GAIN= 29.30DB
TEST3. MEASURED GAIN= 29.32DB
TEST4. MEASURED GAIN= 28.92DB
TEST5. MEASURED GAIN= 28.05DB

UPPER LIMIT OF GAIN = 31.00DB
LOWER LIMIT OF GAIN = 27.00DB

DATA OF AMPLIFIER AMPLITUDE RESPONSE TEST

```
UUT: AMPLN. IC  REV: 4/28/80     .DATE: 5/1/80  9:21.42

MEASURED OUTPUT VOLTAGE1=  207MV
MEASURED OUTPUT VOLTAGE2=  417MV
MEASURED OUTPUT VOLTAGE3=  618MV
MEASURED OUTPUT VOLTAGE4=  774MV
MEASURED OUTPUT VOLTAGE5=  811MV

UUT PASSED LINEARITY TEST
TEST1. MEASURED GAIN=  29.33DB
TEST2. MEASURED GAIN=  29.39DB
TEST3. MEASURED GAIN=  29.28DB
TEST4. MEASURED GAIN=  28.73DB
TEST5. MEASURED GAIN=  27.20DB

UPPER LIMIT OF GAIN =  31.00DB
LOWER LIMIT OF GAIN =  27.00DB
```

DATA OF AMPLIFIER LINEARITY TEST

UUT: OSCAS. IC REV: 4/28/80 DATE: 5/1/80 9:22:58

UPPER LIMIT= 0. 197VRMS

LOWER LIMIT= 0. 155VRMS
MEASURED VALUE= 0. 150 VRMS
UUT FAILED AMPLITUDE STABILITY TEST

DATA OF OSCILLATOR AMPLITUDE STABILITY TEST

UUT: OSCFS.IC REV: 4/28/80 DATE: 5/1/80 9:24.1

UPPER LIMIT= 47760000.0HZ
LOWER LIMIT= 47740000.0HZ

MEASURED VALUE = 47749950.7 HZ
MEASURED VALUE = 47749949.0 HZ
MEASURED VALUE = 47749947.7 HZ
MEASURED VALUE = 47749946.4 HZ
MEASURED VALUE = 47749945.5 HZ
MEASURED VALUE = 47749944.6 HZ
MEASURED VALUE = 47749943.6 HZ
MEASURED VALUE = 47749942.9 HZ
MEASURED VALUE = 47749942.1 HZ
MEASURED VALUE = 47749941.7 HZ
MEASURED VALUE = 47749940.9 HZ
MEASURED VALUE = 47749940.3 HZ
UUT PASSED FREQUENCY STABILITY TEST

DATA OF OSCILLATOR FREQUENCY STABILITY TEST

```
UUT: PWSREG.IC  REV: 4/28/80      DATE: 5/1/80  9:25.56

POWER SUPPLY REGULATION TEST
UUT O/P 1
MEASURED VOLTAGE=    9.03V
UUT O/P 2
MEASURED VOLTAGE=    9.49V
INPUT REGULATION TEST
INPUT VOLTAGE TO UUT= 14.5V
UUT O/P 1
MEASURED VOLTAGE=    9.03V
UUT O/P 2
MEASURED VOLTAGE=    9.50V
INPUT REGULATION TEST
INPUT VOLTAGE TO UUT= 13.5V
UUT O/P 1
MEASURED VOLTAGE=    9.03V
UUT O/P 2
MEASURED VOLTAGE=    9.50V
```

DATA OF POWER SUPPLY REGULATION TEST

UUT: PWSRPL IC REV: 4/28/80 DATE: 5/1/80 9:27:45

RIPPLE MEASUREMENT
UUT O/P1
MEASURED RIPPLE VOLTAGE= 0.001V
UUT O/P2
MEASURED RIPPLE VOLTAGE= 0.001V

DATA OF POWER SUPPLY RIPPLE TEST

UUT: PWSOVC. IC REV: 4/28/80 DATE: 5/1/80 9:28:47

OVER-CURRENT VOLTAGE MEASUREMENT
UUT O/P 1
MEASURED VOLTAGE= 9.03V
UUT O/P 2
MEASURED VOLTAGE= 9.49V

DATA OF POWER SUPPLY OVERCURRENT TEST

```
UUT: MIXFRS1.IC  REV: 3/19/80  · · DATE: 5/1/80  9:30:5

UPPER LIMIT OF IF MEASURED VALUES 1THRU5= 5600.100KHZ
LOWER LIMIT OF IF MEASURED VALUES 1THRU5= 5599.899KHZ

THRESHOLD LEVEL FOR ALL IF MEASUREMENTS=     0.0MV
SELECTED RF= 47750.00KHZ
MEASURED IF=  5600.000KHZ

SELECTED RF= 47900.00KHZ
MEASURED IF=  5600.000KHZ

SELECTED RF= 48100.00KHZ
MEASURED IF=  5600.000KHZ

SELECTED RF= 48400.00KHZ
MEASURED IF=  5600.000KHZ

SELECTED RF= 48850.00KHZ
MEASURED IF=  5600.000KHZ

UUT PASSED FREQUENCY RESPONSE TEST
```

DATA OF MIXER FREQUENCY RESPONSE TEST

UUT: MIXCON1.IC REV: 3/19/80 DATE: 5/1/80 9:32:7

SELECTED RF FREQUENCY= 47750.0KHZ
MEASURED RMS VOLTAGE AT IF OUTPUT= 114MV

SELECTED RF FREQUENCY= 47900.0KHZ
MEASURED RMS VOLTAGE AT IF OUTPUT= 113MV

SELECTED RF FREQUENCY= 48100.0KHZ
MEASURED RMS VOLTAGE AT IF OUTPUT= 114MV

SELECTED RF FREQUENCY= 48400.0KHZ
MEASURED RMS VOLTAGE AT IF OUTPUT= 114MV

SELECTED RF FREQUENCY= 48850.0KHZ
MEASURED RMS VOLTAGE AT IF OUTPUT= 112MV

SELECTED RF FREQUENCY= 47750.0KHZ
CONVERSION LOSS FROM MEASURED VALUES= 15.80DB

SELECTED RF FREQUENCY= 47900.0KHZ
CONVERSION LOSS FROM MEASURED VALUES= 15.89DB

SELECTED RF FREQUENCY= 48100.0KHZ
CONVERSION LOSS FROM MEASURED VALUES= 15.84DB

SELECTED RF FREQUENCY= 48400.0KHZ
CONVERSION LOSS FROM MEASURED VALUES= 15.85DB

SELECTED RF FREQUENCY= 48850.0KHZ
CONVERSION LOSS FROM MEASURED VALUES= 15.99DB

UPPER LIMIT OF CONVERSION LOSS MEAS=20.00DB

UUT PASSED CONVERSION LOSS TEST

DATA OF MIXER CONVERSION LOSS TEST

UUT: FILILO1.IC REV: 3/19/80 .DATE: 5/1/80 9:33:49

MEASURED OUTPUT VOLTAGE= 45MVRMS
INSERTION LOSS= 10.75DB
PER LIMIT= 14.00DB

DATA OF FILTER INSERTION LOSS TEST

```
UUT: FILAMR1.IC  REV: 3/19/80    DATE: 5/1/80  9:35:7

MEASURED OUTPUT VOLTAGE=     3 MVRMS
INSERTION LOSS= 32.66DB
MEASURED OUTPUT VOLTAGE=     4 MVRMS
INSERTION LOSS= 31.20DB
MEASURED OUTPUT VOLTAGE=     5 MVRMS
INSERTION LOSS= 29.04DB
MINIMUM INSERTION LOSS VALUE= 23.00DB
MEASURED OUTPUT VOLTAGE=    36 MVRMS
INSERTION LOSS= 12.72DB
MEASURED OUTPUT VOLTAGE=    45 MVRMS
INSERTION LOSS= 10.78DB
MEASURED OUTPUT VOLTAGE=    47 MVRMS
INSERTION LOSS= 10.52DB
MAXIMUM INSERTION LOSS VALUE= 14.00DB
MEASURED OUTPUT VOLTAGE=    17 MVRMS
INSERTION LOSS= 19.26DB
MEASURED OUTPUT VOLTAGE=    15 MVRMS
INSERTION LOSS= 20.42DB
MEASURED OUTPUT VOLTAGE=    13 MVRMS
INSERTION LOSS= 21.68DB
MINIMUM INSERTION LOSS VALUE= 23.00DB
INSERTION LOSS AT LOWER 3DB PT. =16.47DB
INSERTION LOSS AT UPPER 3DB PT. =17.77DB
```

DATA OF FILTER AMPLITUDE RESPONSE TEST